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A Low-Power Low-Noise Biomedical Instrumentation Amplifier Using Novel Ripple- Reduction Technique

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Abstract-:

This paper presents a low-power low-noise capacitively-coupled chopper instrumentation amplifier (CCIA), which is suitable for biomedical applications such as EEG, ECG and neural recording.A novel ripple-reduction technique combined with ping-pong autozeroing is employed to suppress the ripple at the output of the instrumentation amplifier (IA) by the up-modulated amplifier offset and flicker noise. By using a positive feedback loop in the IA, the IA's input impedance is increased. The complete CCIA is simulated in a standard 0.18 μm CMOS process. The simulated result shows the IA consumes several μA current and 1.8V supply. The equivalent input noise power spectrum density (PSD) is 54nV/√Hz and the noise efficiency factor (NEF) achieves 4.05 within 1 kHz, while the equivalent input noise. PSD is 55.4 nV/√Hz and NEF is 4.15 within 10 kHz. And the input impedance is about 100MΩ.

I. INTRODUCTION-

Recording and monitoring bio-signals such as electroencephalograph (EEG), electrocardiograph (ECG) and neural signals is essential to diagnose diseases including epilepsy, depression, Parkinson's disease and other diseases. EEG and ECG signals lie between 0.5 Hz to 500 Hz and neural signals include local field potential (LFP) and spike potential (SP), respectively from 0.1 Hz to 200 Hz and from 200 Hz to 10 kHz. The amplitudes of these bio-signals range from several μV to several mV. Therefore, before digitising for the backend processing, the instrumentation amplifier (IA) has to have 4060 dB closed-loop gain to amplify the signals from the electrodes with low noise. In addition, low power dissipation is significant to prolong battery lifetime in electronic devices. It challenges the design of the instrumentation amplifier because stringent power and noise trade- offs need to be made. The noise efficiency factor (NEF) is another important figure to assess the performance of the whole instrumentationamplifier.Recentlythe capacitively-coupled chopper instrumentation amplifier (CCIA) topology is widely used in biomedical applications. Chopper modulation is employed to reduce the offset and 1/f noise in low-noise IA, as achieving a flicker noise corner under 1 Hz. But chopper modulation could cause two major problems in CCIA. The first problem is that the up-modulated amplifier offset and flicker noise could result in large ripples at the output. To suppress the ripple, a filter is implemented in and. But using the filter will bring more power consumption and phase delay. A novel technique combined with ping-pong auto zeroing

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technique is used in this paper to suppress the ripple. Besides, with the existing choppers at the input of the CCIA the input impedance is limited by the chopping frequency and the input capacitances of the IA. Considering the specific application environment of biological signals, instrumentation amplifiers require an input impedance of more than 50MΩ. In current feedback instrumentation amplifier (CFIA) structure is proposed.However, good gain accuracy of CFIA requires precise resistance and transconductance matching, which depends on temperature and process.

Biomedical Instrumentation Amplifier

Fig.1 a block diagram of the proposed IA. The system consists of a main amplifier based on ping-pong auto zeroing technique, a transconductance amplifier Gm2 with a class-A output stage, a capacitor negative feedback loop, an impedance boosting loop, an adaptive electrode offset suppression loop, variable miller capacitors Cm1,2, a programmable gain amplifier and the bias pseudo resistors composed by PMOS transistors. Ping-pong auto-zeroing technique combined with DC blocking capacitors CI is employed to suppress the ripple at the output of the IA. The adaptive electrode offset suppression loop made up of integrator and feedback capacitor Chp11,12 is used to compensate for the effect of electrode offset. The input impedance boosting loop is implemented by Cpf1,2 and the choppers CHfb to improve the input impedance of the IA. The variable capacitors Cm1,2 and programmable gain amplifier are used to adjust the gain and bandwidth of the IA to fit different applications for bio signals. Instrumentation amplifier models a crucial part of the low power applications since it demands to individuate noise and small amplitude signal which is desired [10]. The Transforming circuitry resides in an instrumentation amplifier which is applicable for precision amplification of DC/AC signals in differential mode while eliminating common mode signal values [11]. The Well-known design used in a low power sensor system, is an operational amplifier (Op-Amp), must manifest low power consumption and small input voltage referred noise, high Common Mode Rejection Ratio (CMRR). In this proposed work, a low voltage, low noise and high CMRR operational amplifier for a portable monitoring system is described. The proposed op-amp has an innate capacity to work under 1.8-V supply, has required design constraints like high gain & CMRR and low voltage noise [12]. Devices may pertain to different inversion region like weak, moderate and strong Out of these three regions, transistor (MOSFET) functioning in saturation region is most convenient for low power applications where devices are regulated either at low voltage, current or both [13] Fig. 1 shows a typical sensor readout system whose output assumed to be in voltage.The differential voltage (Vid) from the readout system is amplified by the amplifier.

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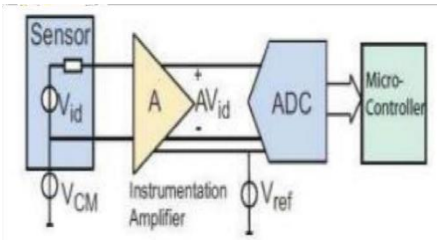

Fig 1.Block diagram of typical sensor readout system As these amplifiers are used to detect very small input differential signals, the input referred errors (due to offset & noise) of such amplifiers should be well below the minimum input signal.

Instrumentation Amplifier

Instrumentation amplifiers can be designed from an op amp circuit but the behaviour of instrumentation amplifiers is intensely different than an op-amp and difficult to design precisely from a single op-amp circuit. Instrumentation amplifiers can be designed in several different ways.The commonly used techniques are difference amplifier, two op-amps, three op-amps, switched capacitor, capacitive coupled, current mode, resistive feedback and current feedback instrumentation amplifier. The classical three op-amp instrumentation amplifier [14] having inputs VIN- & VIN+ defined by the input polarity of the difference amplifier A3. These inputs can be categorised as common mode voltage and difference voltage. Standard instrumentation amplifiers using a unity gain difference amplifier in the output stage, however, can limit the input common mode range significantly [15]. The three op-amp IA suffers from a limited Common Mode Rejection ratio (CMRR) due to resistor mismatch. It does not provide a good power noise trade off; a switched-capacitor IA can be used to improve the CMRR, but it suffers from low input impedance.

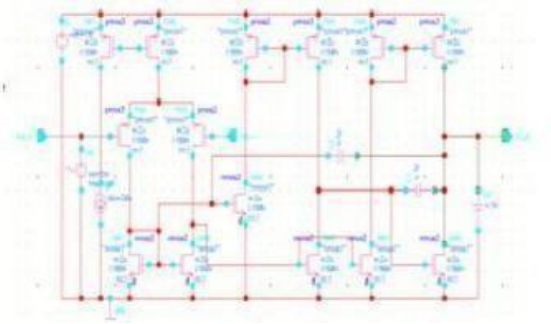

Fig 2 Schematic diagram for three stage amplifier instrumentation

Capacitively-Coupled Chopper Operational Amplifier

A different method to design an instrumentation amplifier is by means of the Switched Capacitor (SC) approach [3]. This kind of technique belongs to the Discrete Time (DT) domain: signals are sampled in precise moments, synchronous with a clock signal, and stored into capacitors. A set of switches (digital MOSFETs in most applications) then moves electric charge from one capacitor to another at every clock edge, in order to achieve amplification. In figure 1.2 is shown a simple example of SC InAmp. This circuit's operation is divided into two phases. During phase 1 (switches with Φ1 closed, others open), input signal is sampled and stored into capacitor C1, while the Op-Amp is in reset state. During phase 2 (Φ2), charge flows from C1 to C2, setting the output voltage. Differential gain is then C2/C1 that is a simple ratio between capacitances: with accurate layout, gain errors of 0.1% are achievable.The strength of this topology is, besides simplicity and area efficiency, a natural Rail-To-Rail input

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CM range, because capacitors block DC voltages, and high CMRR if accurate matching between capacitors is obtained (usually they have excellent matching parameters).

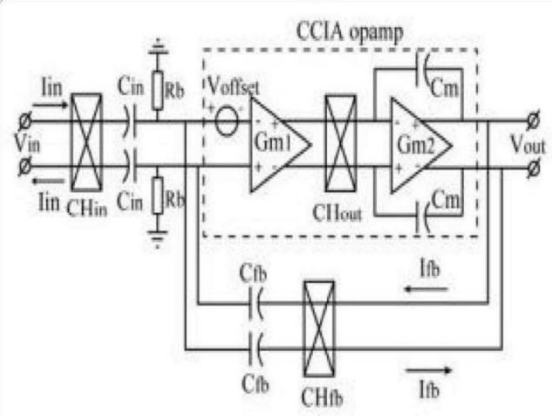

Fig 3 Capacitively-Coupled topology

The CMRR of this topology depends on the matching of the current mirrors and the DC precision of the current mirrors is essential for the overall offset, gain accuracy, drift and linearity. Since the matching of an impedance-boosted current mirror can still be insufficient for the required DC precision, thin-film resistor- degenerated current mirrors can be used in order to achieve CMRR as large as 120 dB [5]. The use of OpAmps as buffers, instead of amplifying elements, extends the input common mode range, though still doesn't include supply rails (unless the two input Op-Amps have true Rail To-Rail output).

Low Power Low Noise Amplifier

Conventional LNA often employs inductive source degeneration. This structure is known for improved noise performance and provides passive matching. However, for limited power budget operation, this structure suffers from low transconductance ( ), impacting noise and gain performance. In addition, a larger inductor would be required for proper matching [13]. In many ULP systems, the popular choice of LNA structure is the inverter-based resistive feedback topology [13]-[14]. As shown in Figure 1, signal is also fed to the active load such that bias current is reused but the gain is boosted by the active loads . It has also been shown in [13] that due to increase, such topology has a better noise figure performance. In [15]-[16], low power consumption was achieved through Ultra-Low-Voltage (ULV) designs at =0.4V and0.5V, respectively.However, the LNA power consumption is about 100µW in both designs.

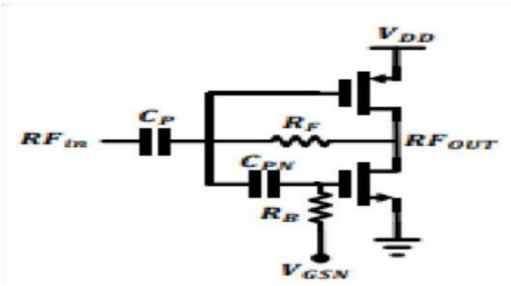

Fig 4 RF/BB Scalable LNA design with NMOS Gate Control

Some general considerations and specifications of LNA suchas noise, gain and power are presented. LNA serves as the first amplification block in a RF receiver

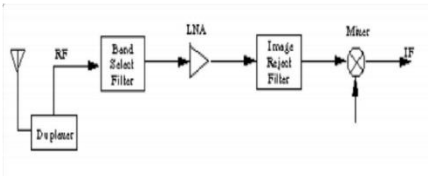

Fig 5 Basic signal receiver system

Figure 1.1 shows an LNA which is used in a heterodyne receiver. While band select filter before the LNA suppress the out-of-band

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interferers, the image reject filter after the LNA rejects the image which is 2ωIF away from the desired band.Even though CMOS technology has been used in digital circuits and low frequency analog circuits for many years, it is only within the early nineties that CMOS is capable of being used in RF circuits. With the backend transceivers already being implemented in CMOS, it is attractive to use CMOS in the front-end in order to integrate the whole receiver on a single chip.An important issue that needs to be taken into account in the design of narrowband CMOS LNA is the high frequency effect. This effect worsens the noise and gain performance of the LNA as will be presented.

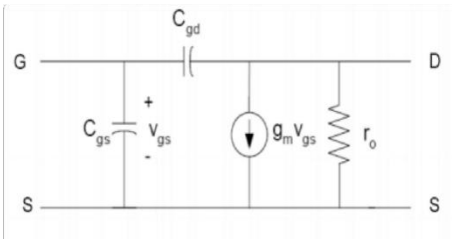

Fig 6 Simple small signal models for MOS at low frequencies

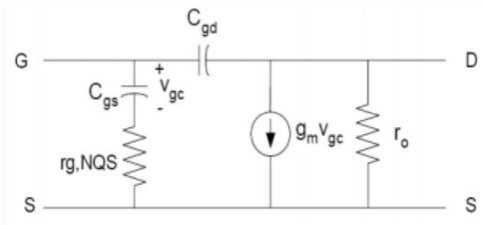

Fig 7 first order small signal model including high frequency effect

Ripple Reduction Technique

Because of the employment of the chopper modulation to reduce the offset and the flicker noise of the IA, the unmodulated offset and 1/f noise of the main amplifier in the CCIA would create a ripple at the output. Assuming the offset *V*os of the main amplifier is10 mV, the transconductance G*m1* of the main amplifier is 10 µS, the chopping frequency *f*chop is 20 kHz and the miller capacitance *Cm1, 2* is 10 pF, the output ripple can be calculated as:

$$= 1 \quad 2 \quad h \quad = \quad , \quad 250$$

This would limit the dynamic range for biomedical signals at the output of the CCIA. Therefore, some methods should be taken to suppress the ripple. This would limit the dynamic range for biomedical signals at the output of the CCIA. Therefore, some methods should be taken to suppress the ripple.

In some applications there is a requirement for better ripple performance than the DC / DC converter can provide on its own. In these instances it is recommended that an external PI Filter be added to the converter's output. The following description is intended as a guideline to design a simple LC filter. Other considerations such as component cost should also be evaluated.The residual offset of the main amplifier in the ping-pong topology will be blocked by the DC blocking capacitors CI. Therefore, the chopper CHm wouldn't modulate the residual offset to a high frequency. The pseudo resistors R21, 22 are formed by

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PMOS transistors working in weak inversion and offer a DC bias for the input of the Gm2 stage.Through this method, the ripple at the output of the IA can be attenuated about 60 dB.Commutation analysis of four-switch inverter shows that the commutation ripple always occur and torque ripple reduction is necessary. Using the direct phase current (DPC) control technique at commutation duration can eliminate the commutation torque ripple in low speed range (case C) in a FSTPI-BLDC motor drive. However, for high speed range (case B) It has been shown that the DPC control method cannot eliminate the commutation torque ripple [8]. Therefore, a novel control technique based on the current slope equalization of two commutated currents is developed

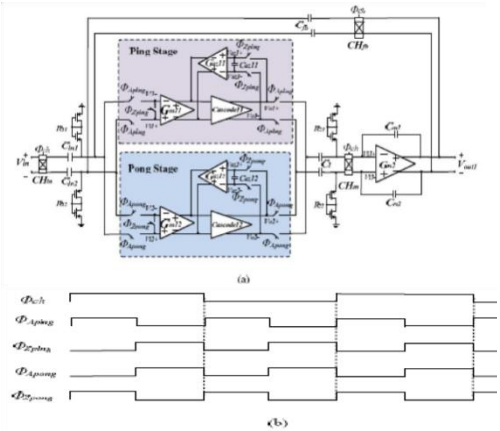

Fig 8 (a) the block diagram of ripple- reduction technique
(b) the timing diagram of ping-pong auto-zero

The direct torque control (DTC) technique of permanent-magnet synchronous motors (PMSMs) receives increasing attention due to its advantages in eliminating the current controllers and quicker dynamic response, compared with other motor control algorithms. However, high torque and stator flux ripples remain in the system when using DTC technologies. This means large stator voltage and current harmonic contents exist in the PM motors. Since the variation of motor electromagnetic torque is related to the voltages that are applied to the motor, by analysing the relationships between stator flux, torque, and voltages, a PMSM torque predictive control scheme is proposed in this paper. In each digital signal processor cycle, the optimised voltage is utilised to reduce torque ripple, and the voltage vector angle is determined by the output of torque and flux hysteresis controllers. The proposed scheme is simulated and experimentally verified. Both simulation and experimental results have shown that low torque ripple and reduced stator current harmonics are achieved by using the proposed scheme.Thus, many studies have been conducted to reduce the vibration and noise in interior permanent magnet motors to ensure improved performance and reliability in electric car drive motors. A variety of papers have introduced methods that reduce the cogging torque and torque ripple. These methods involve adjusting the motor's arrangement, adjusting the width of slots and teeth, using permanent magnet skew, creating auxiliary teeth, using slotless armatures, and using notches [6,7].

PING – PONG Auto Zeroing

The auto-zero technique samples the offset at the output and then uses a negative feedback configuration to an auxiliary input port to cancel the original offset.

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Figure. 2.3 shows the auto-zero technique, by shorting two positive and negative inputs we have Vout = A1 VOS, where VOS is input referred offset voltage, VOUT is the output voltage, and A1 is the dc open-loop gain of the op- amp. Then, the sample-and-hold circuit samples the output voltage and feeds back this value to the input port for cancellation. Since auto-zero technique needs to feedback offset voltage at the output to reduce the input offset voltage and noise, usually there are two phases to realise: sampling and amplifying. In the sampling phase, the input terminals are shorted, so the amplifier is disconnected from the signals and not for amplification use. The input differential voltage is just the dc offset voltage, VOS, and the amplifier will amplify this value, so the output voltage will be set to A1VOS. The sample-and-hold block samples this voltage and then stores it on a capacitor. In the amplifying phase, input terminal

of the amplifier are connected to signals for signal processing, and the stored voltage A1VOS on the capacitor is put into the amplifier's auxiliary input pair to cancel the offset voltage.

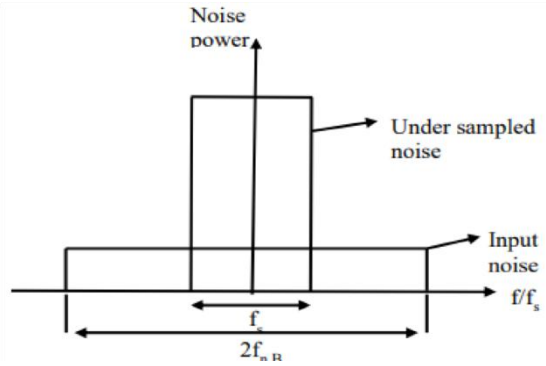

Fig9: Noise spectrum of sampled system

Due to under-sampling, the noise power after sampling increases by this factor as compared to that before sampling (Fig. 2.4), thus incurring a noise penalty. This implies that by choosing a small fn, BW, the folded noise can be restricted. Applying this concept, a slow-settling nulling loop is used to reduce the noise bandwidth to a fraction of the autozeroing frequency. As auto-zeroing involves sampling, it increases noise near DC due to aliasing. Input referred noise PSD of the auto-zeroing technique is shown in

The standard auto-zero transconductance amplifier principle schematic is shown in Figure 2.9 [9, 10]. The base amplifier, Gm1, can either be connected to the input signal or have its inputs shorted together, via S2, S3

II. **Literature survey**:

variable-gainchopper-stabilised instrumentation amplifier (chopper IA),

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which employs low pass filter (LPF) to attenuate the up-converted noise at the chopping frequency, is presented. The circuit is designed and fabricated with Taiwan Semiconductor Manufacturing Company (TSMC) (Hsinchu, Taiwan) 0.18 µm complementary metal-oxide-semiconductor (CMOS) technology. Consuming1.1 mW from a 1.2 V supply voltage, the chopper IA achieves a variable gain of 20.7–48.5 dB, with a minimum bandwidth of 6.7 kHz and a common-mode rejection ratio (CMRR) of 95 dB below 10 kHz. By using the chopper technique, the input-referred noise of the chopper IA can be reduced to 0.28 µVrms (0~96 kHz), with a chopping frequency of 83.3 kHz.An automatic frequency tuning loop (ATL) is employed to adjust the corner Frequency of the LPF dynamically so that the frequency ratio between the chopping frequency and the LPF corner frequency is 8.3, ensuring a noise reduction of 36.7 dB. To meet a variety of healthcare demands, physiological signal acquisition can be performed by implantable, wearable, or portable monitoring systems [1, 2]. Recently, systems that can monitor physiological signals,e.g., electroencephalography (EEG), electrocardiography (ECG), blood pressure and glucose, have been proposed Chopper IAs are widely adopted in these systems for their advantageous low noise, high input impedance, and high common mode rejection ratio (CMRR). The bandwidth of the signal is assumed to be less than half the chopping frequency. The input chopper up-converts the signal to the chopping frequency and its odd harmonics, and then delivers it to the amplifier. After amplification, the signal is then down-converted to its original band by the output chopper.Conventional chopper-stabilised instrumentation amplifier introduces a necessary trade-off between the low residual offset and noise provided by a high transconductance input stage and the resulting high residual ripple. However, to achieve low noise and residual offset, the proposed chopper-stabilised instrumentation amplifier employs a relatively high-transconductance input stage to reduce the offset and 1/f noise, and uses a switched-capacitor notch filter as low- pass filter to filter out the chopper ripple caused by the up-modulated offset and 1/f noise, and introduces a ripple reduction loop (RRL) to reduce the resulting high residual ripple amplitude.

III. Proposed methodology:

The system consists of a main amplifier based on ping-pong auto- zeroing technique, a transconductance amplifier Gm2 with a class A output stage, a capacitor negative feedback loop, an impedance boosting loop, an adaptive electrode offset suppression loop, variable miller capacitors Cm1,2, a programmable gain amplifier and the bias pseudo resistors [2] composed by PMOS transistors. Ping-pong autozeroing technique combined with DC blocking capacitors CI is employed to suppress the ripple at the output of the IA. The adaptive electrode offset suppression loop made up of integrator and feedback capacitor Chp11, 12 is used to compensate for the effect of electrode offset. The input impedance boosting loop is implemented by Cpf1, 2 and the choppers CHfb to improve the input impedance of the IA. The variable capacitors Cm1,2 and programmable gain

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amplifiers are used to adjust the gain and bandwidth of the IA to fit different applications for bio-signals.The main amplifier in pong topology is similar. The noise performance of the proposed CCIA is mainly decided by the main amplifiers in ping-pong topology. Thus, in order to achieve a low noise level, the transconductance Gm11 should be large enough. An implementation of the amplifier to improve the transconductance is proposed. Traditionally, in a folded- cascode amplifier, the current of M2 and M3 will flow into M6 and M7 directly. Considering that there is no need to get a large Gaz11, it's unnecessary to send all the current of M2 and M3 into M6 and M7. Therefore in this schematic, there are two extra transistors M4 and M5 in parallel with M6 and M7. By setting the size of the transistors suitably, the current of M2, 3 is partly reused by M4,5 to improve the effective Gm11 while M6 and M7 form the function of transconductance Gaz11. M2-7 is working at weak inversion to achieve high current transconductance efficiency. The current source provides 1.2 µA to set the equivalent Gm11 as 26 µS and the Gaz11 as 5 µS. The white noise of the main amplifier is about 35 nV/√Hz in the simulation.

IV. Simulation results:

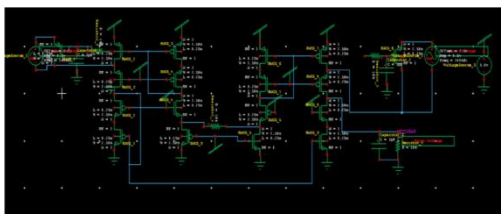

Fig9: Circuitdiagram

```
Device and node counts:
                MOSFETs -       18
        MOSFET geometries -      2
               Capacitors -      3
                Resistors -      4
          Voltage sources -      3
              Subcircuits -      0
        Model Definitions -      2
          Computed Models -      2
        Independent nodes -     35
          Boundary nodes -       4
              Total nodes -     39
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Fig10Circuitdiagram

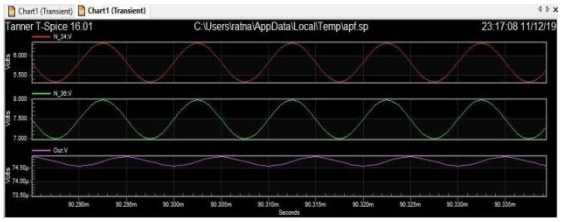

Fig11:Simulationresult

When power is given as 6Amp, we get the output wave as a large amount of current waveform.When we give a small amount of power then we get a small current waveform at the output.Finally it achieves low power consumption and low noise.The overall performance of the proposed CCIA is better than other designs.

V. Conclusion:

A capacitively-coupled instrumentation amplifier for biomedical applications is presented in this paper. This precision IA takes use of ping-pong auto-zeroing technique and DC blocking capacitors to suppress the ripple at the output. An input impedance boost loop is used by the chopper in the negative feedback loop of the first stage to increase input impedance to 100 MΩ. The bandwidth and gain of IA can be programmed from 1 kHz to 10 kHz, 39.9 dB to 59.8 dB respectively to fit different biomedical applications like EEG, ECG or neural recording. It achieves 54 nV/√Hz input referred noise and only 4.05 NEF at 1 kHz bandwidth, 55.4 n V/√Hz input referred noise and only 4.15 NEF at 10 kHz

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bandwidth. The whole IA consumes 3.7µA @1.8V supply.

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