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Performance Analysis of Footed Quasi Resistance Scheme For Low Power VLSI Circuits

G Madhulika(168r1a0478), J Jathin(168r1a0479), J Neelima(168r1a0480),
K Gnaneshwar(168r1a0482)
Department of ECE, C M R Engineering college, Hyderabad, Telangana, INDIA

ABSTRACT-

One of the major problems in cascading dynamic circuits is the logic 1 to logic 0 transition which is solved by using a simple inverter at output named as domino logic. But in domino logic excess power dissipation is observed because of pre charge propagation, which is solved by using a pseudo dynamic buffer (PDB) model. Using PDB we can save almost 67% of power. While succeeding to stop precharge propagation in domino logic PDB allows logic 1 to logic 0 transitions, this may cause erroneous output while cascading. Here we proposed a footed quasi resistance (FQR) model modified from PDB which has advantages of PDB and can avoid logic 1 to logic 0 transitions at output. By using FQR we can get a maximum of 57% power saving compared to domino logic, which is worthwhile to get faultless output in cascaded logic circuits. Simulation is carried out in the O.18Jlm technology node using Tanner EDA tool. Simulation results indicate better performance of modified circuit over conventional and PDB at different frequencies, load capacitance and boolean functions. Keywords-Dynamic Circuits; Low Power Logic Families;Domino Logic; Pseudo Dynamic Buffer; Footed Quasi Resista.

I. INTRODUCTION-

Lately, the rapid advance in multimedia and digital communication systems, real time signal processing like audio signal processing, image and video processing are heavily needed. Many applications such as Processors and Digital Signal Processing operations such as Filtering, Convolutional transformation, require some form of addition such as multiplication, multiply and accumulate operation (MAC) and subtraction.High speed and low power logic circuits are getting more heed in consideration of any device manufacturer. Because of that, many logic families are designed for optimised power and delay . Dynamic logic circuits play predominant roles in present day digital circuits. Dynamic circuit's occupy less area compared with static CMOS circuits. Dynamic logic circuits can be designed with half the transistor count compared with static CMOS logic. Domino logic circuit is modified dynamic logic to avoid erroneous output while designing cascaded dynamic circuits. Domino logic is the same as dynamic logic with an extended static CMOS inverter at the output. Same as dynamic circuits, c1k signal is used to control the operation of domino logic.Dominologic circuit operation divides into two phases. In the first phase, when the clk is low, output parasitic capacitance before static inverter will

ISSN: 2057-5688

charges to Vdd which makes output domino logic output as logic 0 and is called precharge phase and in the second phase, when the c1k is high, load capacitance will discharge or maintain same depending on input and is called evaluation phase. In a domino logic circuit. The 1-bit full adder cell is the main block in all these modules. Because of the need for portable devices such as laptops and cell phones for low power consumption. The power consumption, small area and high speed are the crucial factors to be considered in VLSI design with high performance. There were many techniques to design in VLSI circuit and minimise the power and area, but their best gate diffusion input technique. The aim of this work is to design a 1-bit full adder circuit using full-swing GDI to reduce power consumption, delay and area, in addition to achieving full-swing output.

II. ADDERS

Adders are combinations of logic gates that combine binary values to obtain a sum. They are classified according to their ability to accept and combine the digits. In this section we will discuss quarter adders, half adders, and full adders. A quarter adder is a circuit that can add two binary digits but will not produce a carry. This circuit will produce the following results: 0 plus 0 = 0 0 plus 1 = 1 1 plus 0 = 1 1 plus 1 = 0 (no carry) you will notice that the output produced is the same as the output for the Truth Table of an XOR.X-OR gate can be used as a quarter adder. The combination of gates in figure 1 will also produce the desired results. When A and B are both LOW (0), the output of each AND gate is LOW (0); therefore, the output of the OR gate is LOW (0). When A is HIGH and B is LOW, then (not B) is HIGH and AND gate 1 produces a HIGH output, resulting in a sum of 1 at gate.

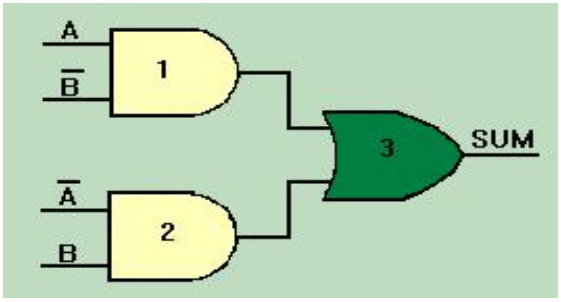

Fig1.:- Quarter adder

HALF ADDER- A half adder is designed to combine two binary digits and produce a carry. Figure 2 shows two ways of constructing a half adder. An AND gate is added in parallel to the quarter adder to generate the carry. The SUM column of the Truth Table represents the output of the quarter adder, and the CARRY column represents the output of the AND gate.

Fig1.2:- Half adders and Truth Table

We have seen that the output of the quarter adder is HIGH when either input, but not both, is HIGH. It is only when both inputs are HIGH that the AND gate is activated and a carry is produced. The largest sum that can be obtained from a half adder is 102 (12 plus 12)

III. FULL ADDER

The full adder becomes necessary when a carry input must be added to the two binary digits to obtain the correct sum. A half adder has no input for carries from previous circuits. One method of constructing a full adder is to use two half adders and an OR gate as shown in figure 3. The inputs A and B are applied to gates 1 and 2. These make up one half adder.The sum output of this half adder and the

ISSN: 2057-5688

carry-from previous circuit become the inputs to the second half adder. The carry from each half adder is applied to gate 5 to produce the carry-out for the circuit.

IV. LITERATURE SURVEY

Tripti Sharma, K.G. Sharma and B.P. Singh, "High Performance Full Adder Cell: A Comparative Analysis",2010 IEEE Students' Technology Symposium 3-4 April 2010,IIT Kharagpur, 2010.Full adder is an essential component for the design and development of all types of processors viz. digital signal processors (DSP), microprocessors etc. Adders are the core element of complex arithmetic operations like addition, multiplication, division, exponentiation etc. In most of these systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is a significant goal. The present study proposes an energy efficient full adder cell with least MOS transistor count that reduces the serious problem of threshold loss.It considerably increases the speed. Result shows 45% improvement in threshold loss problem, 40% improvement in power-delay product over the other types of adders with comparable performance. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm and 130nm technologies.Rajkumar Sarma1 and Veerati Raju," Design and Performance Analysis of Hybrid Adders for High Speed Arithmetic Circuit", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is presented. In this paper, we propose two new designs based on GDI & PTL techniques, which are found to be much more power efficient in comparison with existing design techniques. Only 10 transistors are used to implement the SUM & CARRY function for both the designs. The SUM and CARRY cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using XOR as input SUM as well as CARRY cell is implemented.For Proposed GDI adder the SUM as well as CARRY cell is designed using GDI technique. On the other hand in Proposed PTL-GDI adder the SUM cell is constructed using PTL technique and the CARRY cell is designed using GDI technique.The advantages of both the designs are discussed. The significance of these designs is substantiated by the simulation results obtained from Cadence Virtuoso 180nm environment. A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.Gate diffusion

ISSN: 2057-5688

input (GDI) - a new technique of low-power digital combinational circuit design - is described. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. Performance comparison with traditional CMOS and various pass-transistor logic design techniques is discussed, simulation results are reported, and measurements of a test chip are presented.A. Morgenshtein, I. Shwartz, and A. Fish, “Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process,” 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2010.In this paper CMOS compatible Gate Diffusion Input (GDI) design technique is proposed. The GDI method enables the implementation of a wide range of complex logic functions using only two transistors. This method is suitable for the design of low-power logic gates, with a much smaller area than Static CMOS and existing PTL techniques. As opposed to our originally proposed GDI logic, the modified GDI logic is fully compatible for implementation in a standard CMOS process. Simulations of basic GDI gates under process and temperature corners in a 40nm CMOS process are shown and compared to similar CMOS gates. We show that while having thE same delay, GDI gates achieve leakage and active power reduction of up to 70% and 50%, respectively.’A. Morgenstein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Full Swing Gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.In this paper, the design of a 4-Bit Arithmetic Logic Unit (ALU) using Modified Gate Diffusion Input technique is being done which is implemented using minimum transistor full adder and also adapts hardware reuse method which has advantages of minimum transistors requirement, more switching speed and low power consumption with respect to the conventional CMOS techniques. 4-Bit Arithmetic Logic Unit (ALU) is being implemented with MGDI technique in DSCH 3.5 and layout generated in Micro wind tool. The Simulation is done using 65 nm technology at 1.2 v supply voltage The results show that the proposed design consumes less power and uses less number of transistors, while achieving full swing operation compared to previous work.Larsson, P., & Svensson, C. (1994). Noise in digital dynamic CMOS circuits. IEEE Journal of Solid-State Circuits, 29(6), 655–662.In this paper a general MOS circuit has input signals, internal dynamic nodes and Vdd and Gnd terminals on which harmful noise pulses might appear. A circuit also has internal static nodes on which noise pulses cannot change the logical state. Here we assume that static nodes have a low impedance path to either Vdd or Gnd that will eliminate noise on these nodes generated by sources other than Vdd and Gnd.

V. PROPOSED METHODOLOGY

In 2002 [3] A. Morgenshtein, A. Fish and A. Wagner proposed Gate Diffusion Input Technique (GDI) for low power and small silicon area of VLSI digital design as an

ISSN: 2057-5688

alternative to CMOS logic design. Presented in figure 1 (a) Primitive Proposed GDI cell

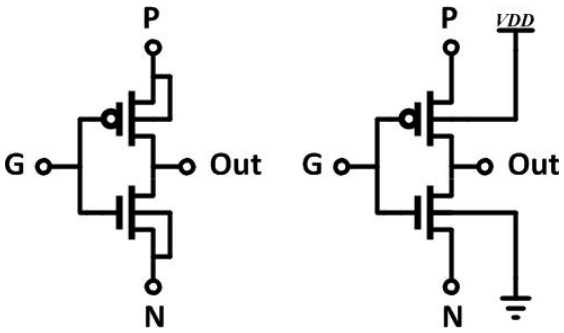

Fig.2:- GDI cell; (a) Primitive Proposed GDI Cell, (b) MOD-GDI

Actually, this technique is proposed for fabrication in silicon on insulator (SOI) and twin-well CMOS processes. Also, it provides an effective way for the design of fast, low power design using less number of transistors as compared to CMOS, PTL and TG techniques.

This allows the design of many complex functions using only 2 transistors as listed in table I. This logic style was suffering from some limitations such as reduced output voltage swing due to the threshold drops, this means that the output either high low voltage is deviated from VDD or GND by threshold voltage drop (Vth), as that threshold drop causes performance degradation and increases short circuit power. To solve this problem Morgenshtein, Shwartz and Fish 4 proposed modified gate diffusion input logic style (MODGDI)the cell is similar to basic cell of GDI, but have important difference in MOD- GDI, the substrate terminals of NMOS and PMOS connected to GND and VDD, respectively, as shown in figure 1(b). This logic is compatible for implementation in a standard CMOS process, and achieves improvement in output, power and power delay product compared to the basic GDI logic. W, while the threshold drop problem, not fully resolved, but the output still has degraded still degrades the output. In [5] Morgenshtin proposed a new approach to improve the output swing and overcome the threshold drop problem known as Full Swing (FS) GDI technique and utilising only swing restoration transistors (SR) to ensure the full swing operation for F1 and F2 function. Either F1 or F2 gates or a combination of both can be used to realise any logical function. Although this technique uses more transistors than standard GDI but compared to CMOS logic style it uses a fewer number of transistors and achieves full swing output, low power, less delay and small area of the circuit.

FULL ADDER- In this paper the Full-Swing GDI technique is used to realise the circuits required to design the Full Adder as follows

XOR GATE-XOR gate is the basic building block for the realisation of various digital circuits such as multiplier, comparator, adder, decoder, and compressor [6]. The design XOR gate requires 4 transistors as shown in fig 2(a). The output can be express as:

At A=0, B=0 the NMOS transistor is switched off and PMOS transistor is switched on, where PMOS in the linear region.At Vin–Vtp<Vout< VDD, NMOS is cut off Vin < Vtn, then the output of XOR gate equal to (Vtp) threshold voltage of PMOS transistor. At A=0, B=1 NMOS is cut off Vin <Vth, the PMOS in the

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linear region Vin– Vth < Vout < VDD, then the output of XOR equal to VDD passes through PMOS. At A=1, B=0 the PMOS transistor is switched off and NMOS transistor is switched on, where PMOS is cut off Vin < Vtp and NMOS in the linear region Vin– Vin <Vout <VDD then the output of the XOR gate is equal to VDD-Vtn, (Vtn) threshold voltage of NMOS transistor At A=1, B=1 PMOS is cut off and NMOS in the linear region, then the output equal to ground passes through NMOS.

VI. SIMULATION RESULTS-

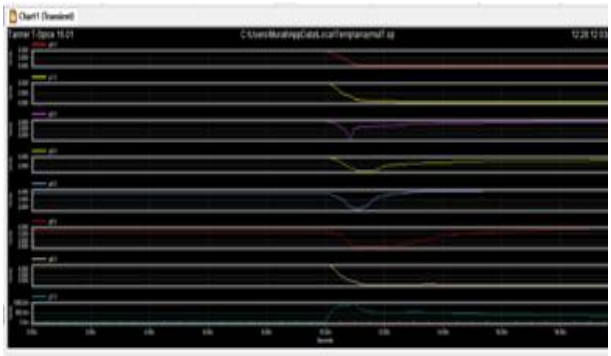

Fig3: Simulation result 1

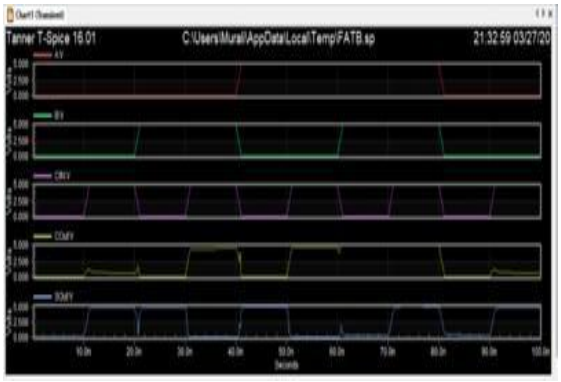

Fig4: Simulation result 2

VII. CONCLUSION

In this paper, we first evaluated the XOR/XNOR and XOR–XNOR circuits. The evaluation revealed that using the NOT gates on the critical path of a circuit is a drawback. Another disadvantage of a circuit is to have a positive feedback on the outputs of the XOR– XNOR gate for compensating the output voltage level. This feedback increases the delay, output capacitance, and, as a result, energy consumption of the circuit. Then, we proposed new XOR/XNOR and XOR–XNOR gates that do not have the mentioned disadvantages. Finally, by

ISSN: 2057-5688

using the proposed XOR and XOR–XNOR gates, we offered six new FA cells for various applications. Also, a modified method for transistor sizing in digital circuits was proposed. The new method utilises the numerical computation PSO algorithm to select the appropriate size for transistors on a circuit and also it has very good speed, accuracy, and convergence. After simulating the FA cells in different conditions, the results demonstrated that the proposed circuits have a very good performance in all simulated conditions. Simulation results show that the proposed HFA-22T cell saves PDP and EDP up to 23, 4% and 43.5%, respectively, compared with its best counterpart. Also, this cell has better speed and energy at all supply voltages ranging from 0.65 to 1.5 V when compared with other FA cells. The proposed HFA-22T has superior speed and energy against other FA designs at all different process corners. All proposed FAs have normal sensitivity to PVT variations.While eliminating precharge pulse propagation, PDB model gets problems in cascaded PDB logic circuits. In this paper we proposed a footed quasi resistance technique which can solve the cascading problem. But in this process we compromise power saving.Which is worthwhile if we consider our proposed technique's advantages over PDB technique. This is observed by taking I-bit full adder circuit power dissipation, delay and Power delay product comparison with traditional domino logic, PDB, and FQR logic models at different clock frequencies and load capacitance. Maximum percentage of power saved by FQR technique is 57%. For fair comparison, power consumption of PDB and FQR is compared with traditional domino logic for different Boolean functions also.

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