INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE

ISSN: 2057-5688

PWM GENERATOR USING VERILOG

Ravi(178r1a04m1), Yadala Vaishnavi(178r1a04m7), Gardasu Aparna(188r5a0406), Anagoni Pavankalyan(188r5a0410)
Department Of ECE, C M R Engineering College,Hyderabad, Telangana, India,

Abstract- Pulse Width Modulation has nowadays become an integral part of every electronics system. These techniques have been widely accepted and are researched extensively nowadays. It has found its application in large number of applications as a voltage controller. Its use in controlling output voltage of Inverter is the most frequently used application. There are basically two main techniques of PWM Generation- Analogue technique and Digital Technique. This thesis deals with these two techniques. First Analogue techniques were studied in detail but these techniques have some demerits. Due to these demerits digital techniques were studied. Various digital PWM Generator topologies were studied. The VERILOG code for each of these topologies was written and synthesized using Xilinx ISE software. Behavioural Simulation was performed on the architecture and after verifying the results this VERILOG code was downloaded to SPARTAN 3E FPGA. After downloading the code in FPGA real time debugging was done for the architecture. The results were seen in ISIM Pro software. Also, from Synthesis report generated after synthesizing the VERILOG code of each digital PWM Generator topologies comparison was done between these topologies in terms of number of logic blocks used and device utilization ofeacharchitecture.

Key words- PWM, VERILOG code, FPGA

I. INTRODUCTION

In Pulse Width Modulation (PWM) has now become an integral part of almost all embedded systems. It has been widely accepted as control technique in most of the electronic appliances. These techniques have been extensively researched during past few years . There are various methods depending upon architecture and requirement of the system. Their design implementation depends upon application type, power consumption, semiconductor devices, performance and cost criteria all determining the PWM method according to N.A. Rahim and Z. Is lams . PWM Inverters are one of those power converters which extensively use concept of PWM for its operation. PWM inverters are recently showing great popularity for industrial applications because of their superior performance. Advancement in designing technology and development in Semiconductor Electronics has led to this popularity.

A numerous PWM schemes are used to obtain variable voltage and frequency supply. According to N.A. Rahim and Z. Islam , there are two classes of PWM techniques identified optimal PWM and carrier PWM. The optimal PWM requires lot of computation and hence extra hardware and hence extra cost.

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE
ISSN: 2057-5688

the disadvantages of these analog methods are that they are prone to noise and they change with voltage and temperature change. Also they suffer changes due to component variation They are less flexible as compared to digital methods. Digital methods are the most suited form for designing PWM Generators.
Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. They are basically interconnection between different logic blocks. When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. We have to just change the interconnection between these logic blocks. This feature of Reprogramming capability of FPGA makes it suitable to make your design using FPGA . Also using FPGA we canimplement design within a short time.
Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. They are basically interconnection between different logic blocks. When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. the disadvantages of these analog methods are thatthey are prone to noise and they change with voltage and temperature change. Also they suffer changes due to component variation
They are less flexible as compared to digital methods. Digital methods are the most suited form for designing PWM Generators. the disadvantages of these analog methods are that they are prone to noise and they change with voltage and temperature change. Also they suffer changes due to component variation. They are less flexible as compared to digital methods. Digital methods are the most suited form for designing PWM Generators.
.

II. Digital Techniques of PWM Generation

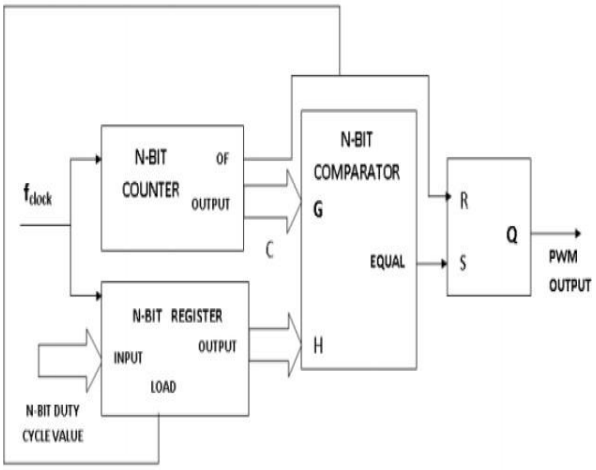
Here, In last two decades, the Pulse width modulation (PWM) techniques are extensively used for controlling the analog circuitry. In particular, it is more commonly used for controlling the power converters employed in various industrial/domestic applications.
In power converters it is used for firing of power electronic devices like thyristors, Insulated Gate Bipolar Transistors (IGBTS), Metal Oxide Semiconductor Field Effect Transistors (MOSFET) etc.[1]-[3]. Inverter fed AC motor drives has wide area of domestic/industrial application. There are many digital techniques available depending upon the arrangement and type of counter used

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE
ISSN: 2057-5688

in this chapter three main PWM Generator topologies are discussed.

High frequency counter based PWM generator

- Counter based PWM generator
- Cascaded Counter based PWM generator



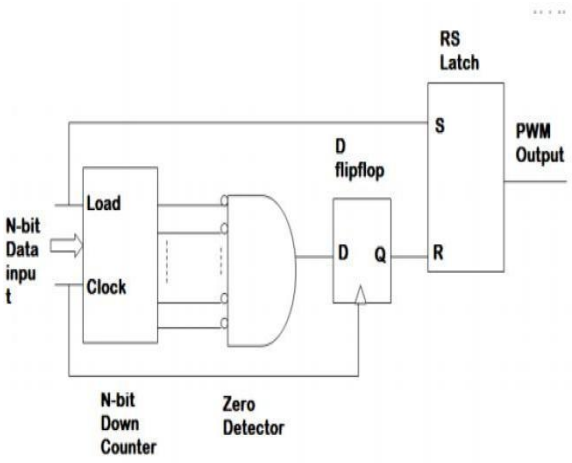


Fig. 3.3: Architecture of Counter based PWM Generator proposed

In this architecture two 4 bit counters are cascaded together to form 8 bits. Than we apply clockto both of counters. We connect the output of both these counters into the 8-bit A input pin ofcomparator. We provide 8-bit input duty cycle to B input pin of a counter.the disadvantages of these analog methods are that they are prone to noise and theychange with voltage and temperature change. Also they suffer changes due to componentvariation . They are less flexible as compared to digital methods. Digital methods are the most suited form for designing PWM Generators

These are we use an Ultrasonic distance sensor, Servo motor and Arduino board. here I am using Arduino Uno. You can also use any other microcontroller. When we place our hand in front of the distance sensor, it will help to the Arduino to measure the distance from the sensor to object (here the hand). if the object in the desired range, Arduino will write the servo to 180. Servo motor is mounded on the hand sanitizer bottle. And the trigger of

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE

ISSN: 2057-5688

bottle is connected to servo by a thread. When servo motor rotates, the trigger will press.

In the semiconductor and electronic arrangement industry, Verilog is a hardware delineation language(HDL) used to show electronic structures. Verilog HDL, not to be mixed up for VHDL (a battling tongue), is most conventionally used in the arrangement, affirmation, and utilization ofdigital method of reasoning chips at the enlist trade level of consultation. It is furthermore used in the affirmation ofanalog and mixed banner circuits. A Verilog setup includes a dynamic arrangement of modules. Modules exemplify layout levels of leadership, and talk with various modules through a course of action of announced data, yield, and bidirectional ports. Inside, a module can contain any mix of the going with: net/variable declarations (wire, reg, entire number, et cetera.), synchronous and progressive decree squares, and instances of various modules (sub- levels of leadership).. Verilog's concept of 'wire' contains both banner regards (4-state: "1, 0, skimming, vague") and characteristics (strong, weak, et cetera.). This system grants calculated exhibiting of shared banner lines, where different sources drive a regular net. Right when a wire has various drivers, the wire's (discernable) regard is settled by a component of the source drivers and their characteristics. A subset of clarifications in the Verilog vernacular is synthesizable. Verilog modules that fit in with a synthesizable coding style, known as RTL (enroll trade level), can be physically recognized by mix programming. Association programming algorithmically changes the (dynamic) Verilog source into a net summary, a really indistinguishable depiction involving just of fundamental method of reasoning locals (AND, OR, NOT, flip-flops, et cetera.).

Beginning Verilog was the principle current hardware depiction vernacular to be composed. It was made by Phil Moorby and PrabhuGoel in the midst of the winter of 1983/1984. The wording for this method was "Electronic Integrated Design Systems" (later renamed to Gateway Design Automation in 1985) as a hardware showing lingo. Entry Design Automation was obtained by Cadence Design Systems in 1990. With the extending achievement of VHDL at the time, Cadence made the lingo available for open systematization. Musicality moved Verilog into the overall public space under the Open
Verilog International (OVI) (now known as Accellera) affiliation. Verilog was later submitted to IEEE and advanced toward getting to be IEEE Standard 1364-1995, ordinarily insinuated as Verilog-95. In a comparable day and age Cadence began the arrangement of Verilog-A to put standards support behind its straightforward test framework Specter. Verilog-A was never intended to be an autonomous lingo and is a subset of Verilog-AMS which wrapped Verilog-95. Verilog 2001 Developments to Verilog-95 were submitted back to IEEE to cover the insufficiencies that customers had found in the primary Verilog standard. These developments advanced toward

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE
ISSN: 2057-5688

getting to be IEEE Standard 1364-2001 known as Verilog-2001. Verilog-2001 is a basic overhaul from Verilog-95. In the first place, it incorporates unequivocal help for (2's supplement) checked nets and factors. As of now, code journalists expected to perform stamped exercises using lopsided piece level controls (for example, the total bit of a clear 8-bit development required an express delineation of the Boolean polynomial math to choose its correct regard). Verilog-2001 is the mind-boggling sort of Verilog reinforced by the predominant piece of business EDA programming packs.Verilog 2005

Not to be confused for SystemVerilog, Verilog 2005 (IEEE Standard 1364-2005) contains minor corrections, spec enlightenments, and a few new lingo features, (for instance, the uwire catchphrase). An alternate bit of the Verilog standard, Verilog-AMS, attempts to organize basic and mixed banner showing with standard Verilog. System Verilog is a superset of Verilog-2005, with various new features and capacities to enable blueprint to check and arrangement illustrating. Beginning at 2009, the System Verilog and Verilog vernacular rules were merged into SystemVerilog 2009 (IEEE Standard 1800-2009). The methodology of gear affirmation lingos, for instance, Open Vera, and Verisity's e vernacular bolstered the change of Super log by Co-Design Automation Inc. Co-Design Automation Inc was later purchased by Synopsys. The foundations of Super log and Vera were given toAccellera, which later transformed into the IEEE standard P1800-2005: SystemVerilog is a superset of Verilog-2005, with numerous new highlights and abilities to help outline check and configuration demonstrating. Starting at 2009, the SystemVerilog and Verilog dialect guidelines were converged into SystemVerilog 2009 (IEEE Standard 1800-2009). The approach of equipment confirmation dialects, for example, OpenVera, and Verisity's dialect supported the improvement of Superlog by Co-Design Automation Inc. Co-Design Automation Inc was later bought by Synopsys. The establishments of Superlog and Vera were given toAccellera, which later turned into the IEEE standard P1800-2005: SystemVerilog. The most beneficial favorable position of SystemVerilog is that it empowers the customer to fabricate strong, repeatable check circumstances, in a dependable punctuation, that can be used over various exercises

A part of the basic features of a HVL that remember it from a Hardware Description Language, for instance, Verilog or VHDL are

There are two separate strategies for announcing a Verilog strategy. These are the constantly and the hidden watchwords. The constantly catchphrase exhibits a free-running strategy. The basic watchword shows a strategy executes accurately once. The two forms begin execution at test framework time 0, and both execute until the complete of the square. Once a constantly square has accomplished its end, it is rescheduled (yet again). It is a run of the mill confused judgment to assume that a fundamental square will execute before a constantly square. Honestly, it is more astute to consider the basic

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE
ISSN: 2057-5688

square a remarkable occasion of the reliably square, one which closes after it completes all of a sudden.

Pulse width modulation (PWM), or pulse-duration modulation (PDM), is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts. The average value of voltage and current fed to the load is controlled by turningthe switch between supply and load on and off at a fast rate. The longer the switch is on compared to the off periods, the higher the total power supplied to the load. Along with maximum power point tracking (MPPT), it isone of the primary methods of reducing the output of solarpanels to that which can be utilized by a battery. The rate (or frequency) at which the power supply must switch canvary greatly depending on load and application. For example, switching has to be done several times a minute in an electric stove. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle. PWM has also been used in certain communication systems where its duty cycle has been used to convey information over a communications channel. In electronics,many modern microcontrollers (MCUs) integrate PWM controllers exposed to external pins as peripheral devices under fir mware control by means of internal programming interfaces. These are commonly used for direct current (DC) motor control in robotics and other applications.
The term *duty cycle* describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on. When a digital signal is on half of the time and off the other half of the time, the digital signal has a duty cycle of 50% and resembles a "square" wave. When a digital signal spends more time in the on state than the off state, it has a duty cycle of >50%. Whena digital signal spends more time in the off state than the on state, it has a duty cycle of <50%. Here is a pictorial that illustrates these three scenarios:

Some machines (such as a sewing machine motor) require partial or variable power. In the past, control (such as in a sewing machine's foot pedal) was implemented by use of a rheostat connected in series with the motor to adjust the amount of current flowing through the Motor. It was an inefficient scheme, as this also wasted power as heat in the resistor element of the rheostat, but tolerable becausethe total power was low. One early application of PWM was in the Sinclair X10, a 10 W audio amplifier availablein kit form in the 1960s. At around the same time PWM started to be used in AC motor control. Of note, for about a century, some variable-speed electric motors.
The signal here the red sine wave is compared with a sawtooth waveform (blue). When the latter is less than the former, the PWM signal (magenta) is in high state (1). Otherwise it is in the low state The simplest way to generate a PWM signal is the intersective method, which requires only a saw tooth or a triangle waveform (easily generated using a simple oscillator) and a comparator.

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE
ISSN: 2057-5688

When the value of the reference signal (the red sine wave in figure 2) is more than the modulation waveform (blue), the PWM signal (magenta) is in the high state, otherwise it is in the low state.

Simulation Output

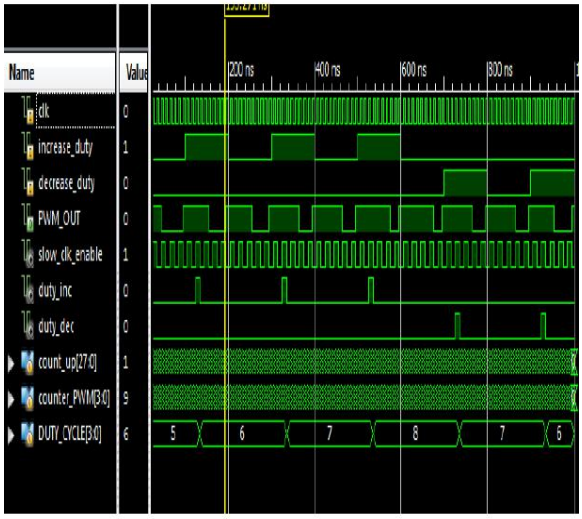
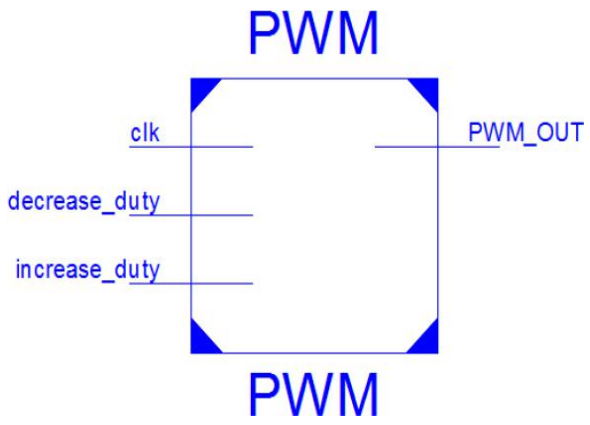
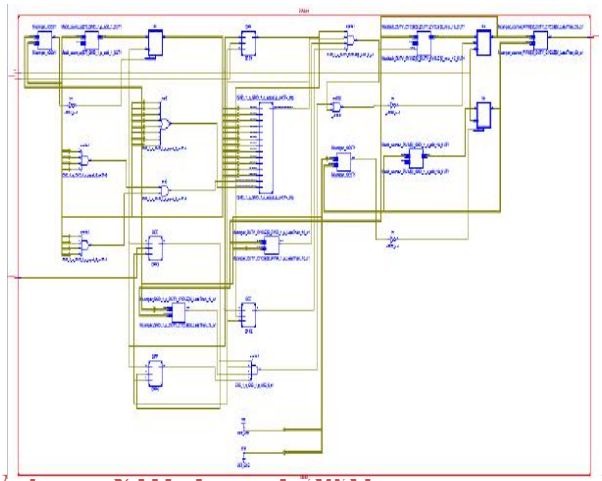


Fig 6.1: Simulation result





Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	12	35200	0%
Number of Slice LUTs	18	17600	0%
Number of fully used LUT-FF pairs	8	22	36%
Number of bonded IOBs	4	100	4%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig 6.1.3: Area Design summary

Conclusion

Various PWM Generator topologies were studied and they were synthesized using Xilinx ISE software. Device Utilization and No of Logic Blocks of each topology were noted down and compared with each other. It was seen that number of logic blocks used in FPGA for design of PWM Generator is minimum in case of Counter based PWM Generator and maximum in case of High frequency Counter based PWM generator. Device (FPGA) utilization is best for Cascaded Counter based PWM Generator and minimum for High frequency Counter based PWM generator. Functional verification was also performed on Verilog code of PWM Generator and simulation was observed. In this study the generation of PWM pulses using Verilog is investigated. A program is developed for the study of PWM generation of fixed frequency in the Verilog which is implemented on FPGA. FPGA are more reliable and suitable than traditional MCUs. RTL schematic validates the output of developed program for Pulse generation. The simulation results showed that an effective PWM pulses can be generated using proposed approach.

Future Work

PWM Generator architecture which was downloaded onto FPGA can be used to control Gate signal of Power Switches of Inverter. By this way we can be able to control ON and OFF time of Inverter. Hence we can use this architecture for controlling Inverter which produces AC from DC source. Hence we can implement PWM Inverter from this FPGA based PWM Generator.The proposed model can be refined and modified for better performance and more accurate PWM generation. The counters can be turned on and off at more précised intervals or instead of counters comparator may be used for the PWM generation purpose in which waveforms can be compared to generate PWM.

REFERENCES

[1] Koutroulis E., Dollas A. and Kalaitzakis K., “High-frequency pulse width modulationimplementation using FPGA and CPLD ICs”, Journal of Systems Architecture , Vol.52 (2006):pp. 332–344
[2] Rahim N.A. and Islam Z., “Field Programmable Gate

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE

ISSN: 2057-5688

Array-Based Pulse-Width Modulation for Single Phase Active Power Filter"; American Journal of Applied Sciences, Vol.6 (2009): pp. 1742-1747

INTERNATIONAL JOURNAL OF TECHNO-ENGINEERING
IJTE

ISSN: 2057-5688

[3] Rashid M.H., Power Electronics Handbook. Florida, Academic Press, 2001
[4] Retif J.M., Allard B., Jorda X. and Perez A, "Use of ASIC"s in PWM techniques for power converters", Proceedings of the International Conference on Industrial Electronics, Control and Instrumentation, IEEE Xplore Press, Maui, HI, USA.,(1993) pp: 683-688. DOI: 10.11.09/IECON.1993.338998
[5] Tzou, Y.Y., H.J. Hsu, T.S. Kuo, "FPGA based SVPWM control IC for 3-phase PWM inverters", Proceedings of the IEEE 22nd International Conference on Industrial Electronics,Control and Instrumentation, IEEE Xplore Press, Taipei, Taiwan, (1996): pp: 138-148. DOI:10.11.09/IECON.1996.570921
[6] Bowes S.R. and Midoun A., "Suboptimal switching strategies for microprocessor-controlled PWM inverter drives", IEE Proc. B. Elect. Power Appli., Vol.132(1985),: pp.133-148. DOI: 10.1049/ip-b:19850