INTERNATIONAL JOURNAL OF TECHO-ENGINEERING
ISSN : 2057-5688

VLSI ARCHITECTURE OF CARRY SKIP ADDERS

* BISAM PRANAYA, ** MOHAMMED RAFI

*MTech student, Dept of ECE, SREYAS INSTITUTE OF ENGINEERING & TECHNOLOGY, Hyderabad, TS, India.

** Assistant Professor, Dept of ECE, SREYAS INSTITUTE OF ENGINEERING & TECHNOLOGY, Hyderabad, TS, India.

Abstract: Adders are key building blocks in the arithmetic and logic units and hence increasing their speed and reducing their power consumption strongly effect the speed and power consumption. There are many adder families with different delays, power consumptions, and area usages. Carry skip adder is efficient in terms of power consumption and area usage, delay also smaller then the ripple carry adder. Carry skip adder allows carry to skip over group of n bits. This paper analyses different very large scale integration design characteristics of various CSK adders in terms of area, power and speed. Based on the detailed review this paper suggests that.

SOFTWARE USED: Xilinx, CSK, Adder, Area, Speed, AND.

1. INTRODUCTION

Carry skip adder is categorized into two types as a single carry skip adder and multi level carry skip adder. Carry skip adder is low cost adder because x-bit carry skip addition is portioned into m= $\sqrt{x}$ blocks. There blocks require only AND gates and multiplexers. However, the performance lags a compared with other adder structures.

There carry skip adders can be implemented by using field programmable gate array for low power applications by using less number of resources.

Adders are used as a basic and important part of an arithmetic and logic operation or arithmetic and logic unit (ALU) [1].Arithmetic and logical units are widely used in microprocessors, microcontrollers, data processing unit and digital signal processing. Adder is also used for different binary operations like multiplication, subs traction division, complements (2's and 1's) decoding, encoding, and so on [2]. Therefore, adder plays an important role in central processing unit (CPU).generally, arithmetic and logical operation performs slowly on compared with other processors operations. So the adder performance fixes the optimum frequency of operation of any processor chip. Also any light speed adder can increase the performance of any chip [3].

The simplest addition operation is the ripple carry adder. The hardware architecture of their adder is very simple but the delay in this adder the increases linearly by increasing

ISSN : 2057-5688

number of bits[4].Various hardware architecture have been implemented to improve the performance of adder in the past decade. Different high speed adders are carry-look ahead adder, carry select adder and carry-skip adder.

This work examines the design and implementation of various skip-adder architecture by using FPGA technology.

This synopsis is structured on follows; section 2 describes the detailed survey on carry skip adder. Section 3 and 4 provide problem statement and objectives respectively. section 5 brief the proposed method and section 6 schedules the implementat

2. Literature Survey

S.No.	Title Name	No. of Transistors / Area / Gate Count / LUT's	Speed\delay	Power
1.	Design and Implementation of 4 bit carry skip adder using NMOS pass transistors logic (Vishal bharat et.al., 2017)[23]	Area 35.2% reduced	Delay 60% reduced	N/A
2	Implementation of carry skip adder using pass transistor (Sridevi, 2017)[6]	No. of transistors 472 Area 27 μm^2	Delay 136.8 ns	351.2mW
3.	Implementation of high speed 32-bit carry skip adder using concatenation and incrimination logic (Mahesh et.al., 2016)[27]	N/A	Delay 19.096ns	N/A
4.	Partially duplicated code-disjoint carry skip adder (V. Ocheretni et.al., 2002)[25]	Area 33.4%	31%delay reduced	5.5%
5.	High Speed self-timed carry skip adder (A. Amin, 2006)[11]	No. of transistors 118	Delay 0.87 ns	Power 2.2
6.	A New 16 bit high speed and variable stage carry skip adder(anjali,2017)[28]	N/A	Minimum speed	N/A
7.	Delay Optimization of carry skip adders and block carry look ahead adders using Multidimensional dynamic program (chann,1992)[16]	N/A	Minimum Delay	N/A
8	High speed self timed carry skip adder,(amin ,2006)[11]	Area 220nm	n\a	n\a

9	Enhancing the efficiency of carry skip adder using MBFA-10T(K.Kumaran,2017)[8]	Transistors 36	N\A	N\A

Chirca et al (2004) [24] proposed a high performance 32-bit carry skip adder by dividing the overall addition operation into variable sized blocks. This utilizes carry look ahead logic to reduce the propagation carry and to reduce the overall delay. The architecture of this carry skip adder is implemented on 130nm CMOS technology and the performance of this method is compared with different high performance adder. This carry skip adder works with 71.2ps and 0.786mw power, further the delay is this CSA is less than some other adders like ripple carry adder, carry increment adder. However the performance of this adder is poor on compared with carry propagate adder.

Michael et al (2004) [26] proposed a low power carry skip adder with fast saturation. This method uses variable sized blocks .This blocks balance the delay of inputs to the carry chain. In general, the adder architecture decreases power consumption by reducing the number of transistors, logic levels, and glitches. This carry skip adder is implemented by using 130nm CMOS technology. This 32 bit carry skip adder works with 600 MHz with the delay of 12.9 ns.

Sridevi et al [6] (2017) implemented a carry skip adder using pass transistor logic. This implementation uses PTL to enhance the parameters like area, power and delay this is implemented by using cadence virtuoso 61.4 software at 90m technology. By comparing with other conventional CSK, this implementation provides optimized result on number of transistors is 472 and power consumption is 351.2mw but the conventional CSK uses 472 transistors and consume 494,1mw power.

Vishalbharat et al [23] (2017) proposed a carry skip adder using NMOS pass transistor logic. This design uses NMOS pass transistor logic it is implement by using cadence RTL front end design tool, 180 nm. This architecture reduces area by 35.2 µm and delay is reduced to 60%.

Ocheretnit et al (2002) s[25] proposed a self checking code disjoint fast carry skip adder for 64bits. This adder is fastest self checking adder, in this design instead of a single carry in signal of the adder cells ,the carry signal is split into two different signal lines. In this design the propagate signals are implemented only once, there are utilized to compute the duplicated sum bits and simultaneously to check the input parity and some internal XOR

ISSN : 2057-5688

gates. This design outperforms other self checking disjoint carry look-ahead adders with maximum delay, area and power reduced to 31%, 33% and 5.5% respectively.

Mahesh et al (2002) [27] designed a high speed 32-bit carry skip adder using concatenation and incrimination (CI) logic. This design utilizes AND-OR-invert and OR-AND invert compound gates. This method CI-CSK shows a higher speed compared with the other adders. Further, the CSK is realized with both fixed size and variable stage size, the speed improvement is achieved by using variable size blocks, parallel prefix adders in nuclear stage. This implemented adder is compared with the other adders its delay is low, that delay is 19.046ps.

Vijayan[2] et al (2012) proposed different adder topologies. The adder structure an implemented by using 0.12 um technology. By comparing different topologies the CSA adder topologies uses least gate count

Amin et al (2006) designed an efficient self timed carry skip adder with low area overhead and fast operation. In this design the adder completion detection circuit used based on a simplified realistic process tracking bounded delay model, it achieves less area overhead and fast completion compared with the other self timed adder. This circuit is more efficient in terms of speed and area, the architecture is implemented by using self timed carry skip adder works of 0.87ns and with supply voltage 1.8v

Arora et al (2017) [28] provided a 16 bit high speed and variable stage carry skip adders this adder is simulated using 90 nm CMOS technology in cadence virtuoso, this design consists of seven stages, the first and last stages are contains 1 bit each, and it is increasing steadily till the middle stage. This design reduces power consumption by 8% and reduces the delay by 61.75%.

Mincha et al[3] (2000) implemented a modified carry skip adder for reducing first block delay. This implementation utilizes carry look ahead logic and it is used for the first carry computation. This technique is certainly works well with fixed size blocks. The modified carry skip adder compared with the other adders the modified carry skip adder uses extra gates because of carry look-ahead logic this adder works of 1.4ns.This adder is useful in the small bit addition.

Manasa et al (2017) designed a high speed and energy efficient carry skip adder, by using AND-OR-invert and OR-AND-invert compound gates for the skip logic. In this design both fixed size and variable stage size styles are used, the speed enhancement is achieved by

ISSN : 2057-5688

the modifying the structure through concatenation and incrimination techniques. The total delay of this carry skip adder is 15.61ns.

Guyot et al (1987) [19]built a efficient carry skip adder by using blocks of variable sizes this is a two level carry skip adder which is implemented on microcomputer using VLSI technologies (2µm gate CMOS).The computing time of the 128 bit adder is approximately 50ns.This performance of this carry skip adder is higher than other adders like ripple carry adder and carry look ahead adder.

Burgers et al (2001)[3] described a modified carry skip adder to reduce the propagation delay by using skip multipliers. The skip multiplexer is used to replace most significant blocks (MSB) by a carry select adder stage. This carry-skip adder increases the speed of operation by comparing with single-level carry-skip adder. For instance, this accelerated CSK produce 25gate delays for 64 bit addition but the single-level CSK uses 30 gate delays to perform the same 64 bit addition operation.

Bahadori et al (2015) [1] designed a carry skip adder structure and compare the higher speed and lower energy consumption with the conventional one. Instead of using multiplexer logic to use AND-OR invert and OR-AND invert compound gates for skip logic. This design use the variable latency extension, which is lowers the power consumption without considering the speed. This extension used the modified parallel structure for increasing the slack time. This adder use improve the energy is 38%, and reduced the delay is 44%.

3. Problem Statement

Based on the survey we observe on the conventional carry skip adder uses more number of ripple carry adder blocks, more number of gates so increase the area, power and delay.

1. In that conventional CSK adder to use more number of gates used so increase the area.
2. Use the single level carry skip adder blocks increase the delay

4. Objectives

1. To accumulate an extensive understanding of architecture of carries skips adder and the realization in FPGA.
2. To identify suitable algorithm for further improved by means of their performance (speed)
3. To increase the speed of operation by multiple level carry skip logic and variable size block
4. To compare the performance of different kind of carry skip adders

5. Proposed Method

ISSN : 2057-5688

Instead of using multiplexer logic to use multilevel carry skip blocks and variable size blocks are used to increase the performance, by using concatenation.

The proposed structure makes use of AND OR invert and OR AND invert compound gates for the skip logic so reduced the area and delay.

In this method the logic replaces 2:1 multipliers by AOI and OAI compound gates. Its consists of fewer transistors, and lower delay, area and power consumption.

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries, their inverter gates are used to increase the power consumption and delay is eliminated

To reduce the delay and power consumption by using variable sized blocks to balance the inputs to the carry chain, further reductions in delay are achieved by using complementary carry logic in the carry chain.

Further this work suggests enhancing the delay characteristics by using optimal block size to perform carry-skip.

CONCLUSION

Based on the survey we observe on the conventional carry skip adders uses more number of ripple carry adder blocks,more number of gates so increase the area, power,delay.

1. In that conventional CSK adder to use more number of gates used so increase the area.
2. Use the single level carry skip adder blocks increase the delay

REFERENCES

1. Bahadori M. Kamal M.Kusha A. and Pedram M,"High-speed and energy efficient carry skip adder operating under a wide range of supply voltage level", IEEE Transcations on VLSI systems,2017.
2. Sridevi " Implementation of carry skip adder using pass transistor logic" international research journal of engineering and technology, pp2201,2017.
3. Michael J. Schulte. Chirca K. Wang H.Balzolo P."A low power carry skip adder with fast saturation",procedding of the IEEE international conference on application, specific systems on architecture and processors,2004.
4. Amin A, "High speed self timed carry skip adder" , The institution of engineering and technology IEE proc- circuits devices syst. vol.153 NO.6, pp574-578,2006.

ISSN : 2057-5688

5. Vishalbharath. Hakki,"carry skip adder using nmos pass transistor logic", international journal of of computer science and mpbile computing,pp.203-207,2017.
6. Chirca K.Michael S.Glossener J."Static low power high performance 32-bit carry skip adder"conference paper January 2004.
7. V.Ocheretni"partially code disjoint carry skip adder",IEEE international symposioum on defect and fault tolerance in VLSI system,2002.
8. P.K. Chan et al., "Delay Optimization of Carry-Skip Adders and Block Carry-Look a Head adders Using Multidimensional Dynamic Programming," *IEEE Trans. Computers*, Vol. 41, No, pp. 920-930.8 august 1992.
9. Mahesh P. Sravanthi R, "Implementation of high speed 32- bit carry skip adder using concatenation and incrementation logic", international advance research journal in science, engineering and technology, pp.198-201,2016.
10. Anjali A.Vandana N, " A NEW 16 bit high speed and variable stage carry skip adder", 3rd IEEE international conference on computational intelligence and communication technology,PP.1-4,2017.
11. Michael J. Schulte. Chirca K. Wang H.Balzolo P."A low power carry skip adder with fast saturation",procedding of the IEEE international conference on application, specific systems on architecture and processors,2004.
12. signa Jom,asha J,"IEEE international conference on circuits and systems in digital enterprise technology,2018.
13. Santhosh NS,Shivarudraiah M.R,Amaresha SK,"international journal of engineering and advanced research technology,volume -4,p.p1-4,may 2018.
14. Guyot,B.Hochet,and J.M.Muller," A way to build efficient carry skip adders",IEEEtrans. computers,pp 1144-1152,oct 1987.
15. P.K.chan and M.D.F Schlag"Analysis and design of CMOS Manchester adders with variable carry skip adder "IEEE trans.computers no.8,pp 983-992,aug1990.
16. P.K Chan "Delay optimization of carry skip adders and block carry look ahead adders using multidimensional dynamic programming," IEEE trans computers,pp 920-930,august 1992.
17. Chirca K.Michael S.Glossener J."Static low power high performance 32-bit carry skip adder"conference paper January 2004.

ISSN : 2057-5688

18. Mahesh P. Sravanthi R, ”Implementation of high speed 32- bit carry skip adder using concatenation and incrementation logic”, international advance research journal in science, engineering and technology, pp.198-201,2016.

19. Anjali A.Vandana N, ” A NEW 16 bit high speed and variable stage carry skip adder”, 3rd IEEE international conference on computational intelligence and communication technology,PP.1-4,2017.