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A NOVEL MIXED MODE SCAN DESIGN WITH EFFICIENT SCAN FLIP FLOP ARCHITECTURE

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Abstract: The performance burden of scan designs is caused by the scan multiplexers that are added to the inputs of each flip-flop. In today's high-speed plans with the lowest possibility of combinational depth, the performance loss caused by the scan multiplexer has increased. To keep the circuit's performance, the overhead in the timing of the design scan has to be addressed. The new scanner f/f-based, weighted self-test built into the circuit (BIST) method is proposed using a weighted pseudorandom test pattern generation. We offer the design of a new flip-flop scan, which eliminates the cost of serial scanning. The method proposed eliminates the scan multiplexer out of the operational path. The proposed design will assist in enhancing the frequency of operation of techniques that are performance-critical. In addition, the proposed method could be utilized as a typical scan flip-flop during a "mixed scan" test wherein it could be used as a serial scan cell and a Random Access Scan (RAS) cell. A mixed scan tests design was implemented using the scan flip-flop concept. The experiment results show an impressive decrease in the length of the interconnect wire and test duration and test data volumes, as contrasted with the most advanced random access scan and multiple scanners implemented in serial mode. In the pseudorandom testing phase, the weighted random test pattern generation technique is proposed through the deactivation of the scan chain.

Keywords--Scan flip-flop, Serial scan test, weighted test-enable signals, Random access scan test, mixed-mode scan test, Low power test, Test application, time, Test data volume.

1. INTRODUCTION

The performance of electronic equipment and gadgets has experienced enormous growth over the last two decades. Moreover, their weights and sizes have decreased dramatically. The main reason for this is the rapid technological developments that allow the fabrication of millions of transistors on an integrated circuit (I.C.) or chip. Each I.C. that is used in the market follows Moore's law. By Moore's direction, the amount of transistors (transistor density) within an I.C. increases by a factor of 1.5 years. As technology advances technology, the device shrinks to nanometer size.

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However, the thickness and the complexity of I.C.s keep increasing. This can lead to a variety of malfunctions in the manufacturing process and even device failures. To allow for more transistors, the features are reduced in size. Reduced feature sizes mean that the manufacturing process is more susceptible to errors and detecting faults becomes extremely difficult. VLSI tests are becoming increasingly crucial and challenging to determine whether the device functions correctly or not. The traditional automated tests equipment (ATE) tested technique is no longer adequate to meet the increasing testing challenges.

Logic built-in self-test (LBIST) is widely adopted as the testing technique for most current scan-based designs. Logic BIST does not alter the scan structure of the methods permitting them to have both ATE based testing and Logic BIST. The nature of vectors in Logic BIST are usually pseudorandom, so even for a moderately sized design, several thousands of patterns are to be generated in the Logic BIST compared to a few hundreds of deterministic test patterns in ATPG to achieve adequate fault coverage. So, methods to improve the fault coverage of Logic BIST by increasing the pattern efficiency are constantly explored.

LBIST found its use mainly in safety-critical (automotive, medical, military), mission-critical (deep-space, aviation) and high-availability (telecom) applications. However, process technologies plunging below 22nm, LBIST will become compulsory for application-specific integrated circuits (ASICs), application-specific standard products (ASSPs) and complex commercial I.C.s (Nan Li et al., 2015). Any electronic system employed in safety-critical applications is expected to have a periodical self-testing scheme for sustained error-free operation. For example, electronic medical devices need to test themselves to assure the continued safety of the patients. Another example is automotive electronics. With the explosion in the growth of the automotive semiconductors industry comes an associated and intense focus on high silicon quality and reliability. The last thing anyone wants is a brake 3 system failure due to a latent silicon defect, and concerns over reliability are driving changes in the testing requirements for these chips. Electronics must meet specific safety standards to accommodate the fast-growing technological revolution.

There are various flip-flop structures even for the same type of flip-flop. However, they operate similarly and are obtained by cascading two latches, each showing input logic values at one of the two clock phases (clock = 1 and clock = 0). One of a scan cell implementation and bits based circuit as shown Fig 1. It is a positive edge triggered mixed input D flip-flop (M.D. flip-flop) whose transition. The course highlighted by the dashed rectangle is the multiplexer used for selecting between the functional data-in (D) and test scan-in (T.I.) inputs. The circuit

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between the nodes D.P. and M.D. is the master latch of the flip-flop, and this is connected to the slave latch, the circuit between the node M.D. and the output (Q). When the test enable signal (T.E.) is set to 1 (0), T.I.

(D) Is selected. The value of T.I. (D) then propagates into the master latch when the clock (C.P.) is low. Meanwhile, the nodes in the slave latch retain the values from the previous clock cycle. When CP turns to high, the signal stored in the master latch propagates into the slave latch and to the output of the scan cell.

Built-in Self-Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their operation (functionally, parametrically, or both) using their courses, thereby reducing dependence on external automated test equipment (ATE).

The main drivers for the overall development of BIST techniques are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed-signal testers that possess exceptional digital and analogue testing capabilities. BIST can perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high-end testers.

BIST is also the solution to critical testing circuits with no direct connections to external pins, such as embedded memories used internally by the devices. Shortly, even the most advanced tester may no longer be adequate for the fastest chip, a situation wherein self-testing may be the best solution.

Advantages of implementing BIST include: 1) lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated; 2) better fault coverage since unique test structures can be incorporated onto the chips; 3) shorter test times if the BIST can be designed to test more structures in parallel; 4) more accessible customer support, and 5) capability to perform tests outside the production electrical testing environment. The last advantage mentioned can allow the consumers to test the chips before mounting or even after they are in the application boards.

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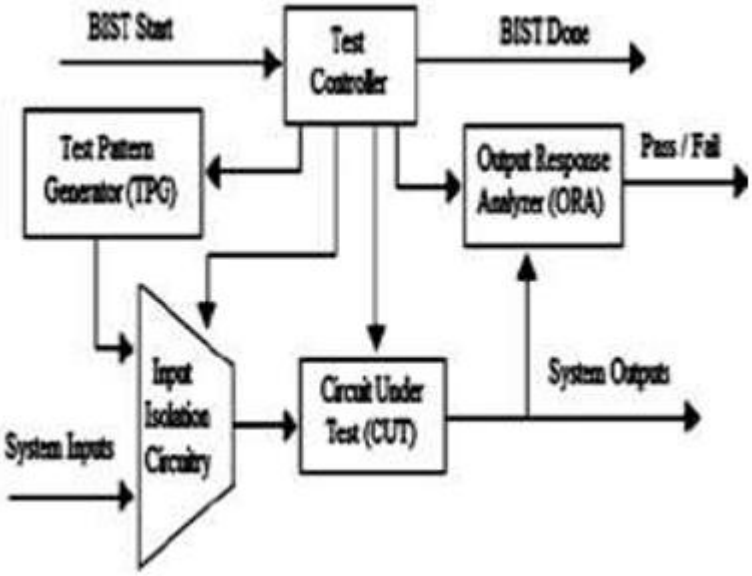

Fig 1: bits based circuit

BIST allows a hierarchical breakdown of cascaded devices for testing purposes. Example A board with only a few chips: The system sends an indication to the board that activates BIST on the chip in the chip. Results are transmitted into the plans. In the event of an error, BIST hardware will indicate the defective component. BIST tests all integrated designs as well as interconnects. It leaves only the functional testing that the plan is cascaded for system-level tests. Test generation, practically impossible to carry tests and responses involving hundreds of chip inputs through many layers of circuitry to chip-under-test. BIST localizes testing, eliminating these problems. Test application BIST saves significantly try application time compared to external testers z BIST testing capabilities grow with the VLSI technology. In contrast, test capabilities always lag behind VLSI technology for external testing z Low development cost, as BIST is added to circuits automatically through CAD tools.

II. RELATED REVIEW

Scan Flip-Flop Design

A serial scanner is not entirely free of negatives. Some inherent disadvantages are associated with this type of scan. The penalties are: 1.) overhead for performance, 2) the volume of test data, 3) testing power consumption and four) testing application time. Scanning multiplexers cause the performance overhead associated with serial scans. The scan multiplexer fits into each clocked pathway and imposes an additional performance penalty of about two gates of delay. A circuit that is not designed with the scan and one with the scan design is depicted in the fig.

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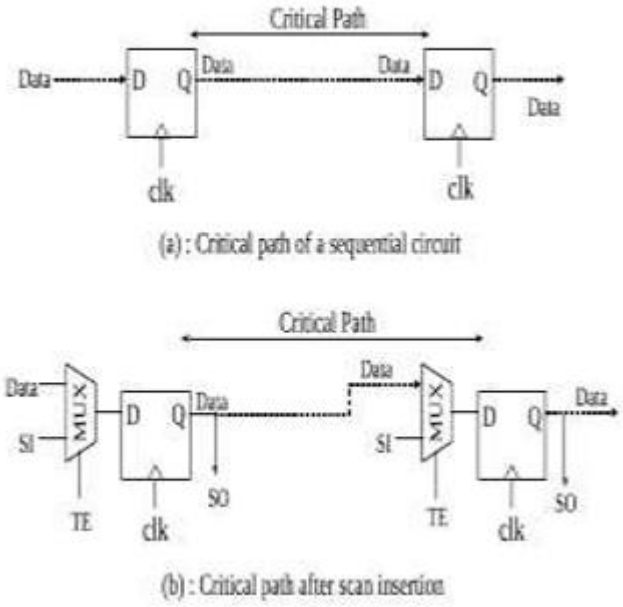

Fig 2: critical path of a sequential circuit

As observable in Fig 2(a), the critical path of a sequential circuit without scan insertion is decided by the longest combinational path between two flip-flops. However, in a scan inserted sequential circuit (see Fig 2b), the same critical way is elongated by a scan multiplexer at the end of the combinational path. The scan design also adds an extra fan out at the output of a flip-flop. These factors increase the critical path delay, hence reducing operating clock speed by 5% to 10%. This makes it necessary to eliminate the performance overhead of the scan multiplexer.

Several solutions have been proposed to alleviate the performance penalty of scan design. One such solution that helps the performance overhead and the other fines associated with the serial scan design is the use of partial scan instead of complete scan. In partial scan design, only subsets of all flip-flops in Circuit-Under-Test (CUT) are replaced by scan flip-flops to form a scan chain. This subset does not include flip-flops of the critical paths, hence reducing the performance penalty of the scan.

Additionally, the partial scan design techniques also reduce test data volume and test application time directly related to test cost. However, the partial scan design techniques may lead to lower fault coverage of the CUT. The selection of flip-flops in partial scan design can be testability measures based, structure-based, or ATPG based. The structure-based techniques select flip-flops to cut off the feedback path. These techniques use heuristics based on network topology for determining a minimum set of flip-flops and do not explicitly analyze the circuit behaviour. The ATPG based methods select flip-flops that are useful for test generation. These

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techniques first use sequential ATPG to generate test vectors for all possible faults. The related flip-flops are found for the scars that remain undetectable, and these are included in partial scan design.

Most partial scan techniques require computationally demanding sequential ATPG and cannot be afforded with ever-increasing circuit complexity. Furthermore, partial scan design techniques do not provide as high fault coverage as the complete scan design offers, and it is challenging to integrate them into the existing industrial design flow. Another approach for eliminating the performance penalty of scan design is to use scan cell designs that provide high performance. Galbi et al. proposed a dual-edge pulse-triggered scannable flip- flop which is a high performance and low power scan cell. In recent work, Satyadev. Use a modified scan cell wherein the scan multiplexer is eliminated from the functional path by using a separate master latch for useful and test mode. These high-performance scan cell designs can eliminate the performance overhead of scan design. However, such scan cells cannot be used in a mixed scan test architecture.

Random access scan (RAS) is an alternative DFT technique that can alleviate the problems associated with the serial scan. Literature shows that RAS can significantly reduce test application time and test data volume along with test power reduction. However, the hardware overhead associated with RAS is prohibitively high. The routing congestion due to interconnect wiring is a severe issue that impedes the practical Implementation of the RAS. In the recent past, Baik. They proposed some innovative changes to the basic RAS architecture to overcome the routing congestion issue. Baik et al. offered an improved version called Progressive Random Access Scan (PRAS) design to improve test time and routing wire length.

The PRAS design uses separate row and column address decoders in place of a single address decoder. The same authors have shown that the arrangement of RAS cells in a square grid of size p N p N is optimal for improving routing congestion, where N is the number of scan cells. Mudlapur et al. further address the routing congestion problem by eliminating the scan-in and test-enable lines. However, it introduces an additional gate delay in the clock path due to clock gating. Adiga et al. proposed a modified T flip-flop design to eliminate the clock gating introduced in the clock tree. Despite these efforts, routing congestion is still a critical issue that needs to be resolved to make RAS Implementation practical.

Furthermore, observability of storage cell and RAC architecture implementation are other issues that need to be adequately addressed. The first step in mixed mode scan architecture implementation is the segregation of all the flip flops into two groups. One group of the flip-flops is assigned to the serial port and the flip-flops from the second group go into the RAS part. The

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segregation of scan cells among serial features and the RAS part is very crucial for test time, test data volume, test power dissipation, and area overhead. For the current work, we have used a simple criterion based on test pattern care bits. The scan cells for which most of the patterns are specified with care bits are included in the serial scan part, whereas those scan cells.

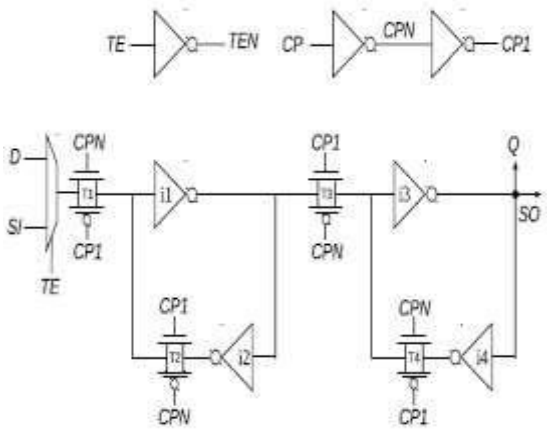

Fig 3: A conventional scan flip-flop design

A conventional scan flip-flop design is shown in Fig 3. This scan cell is a master-slave latch based positive edge-triggered mixed input D type flip-flop. The transmission gate T1 and the inverter pair connected back to back via transmission gate T2 forms the master latch. The slave latch comprises transmission gate T3 and the inverter pair connected back to support via transmission gate T4. The multiplexer at the input of master latch selects between functional input (D) and scan input (S.I.) depending upon the value of test control signal test enable (T.E.). In test mode, when T.E. is high (1), S.I. is selected and is connected to the master latch's input. When the clock signal (C.P.) is low (0), the value of S.I. propagates to the master latch. In the meantime, the slave latch retains the value from the previous clock cycle. The value latched into the master bears to slave latch when C.P. turns to high (1) and the output Q of scan flip-flop.

Similarly, when the test Enable signal (T.E.) is set to 0, functional input D is selected, and the circuit operates in active mode. The architecture of the mixed-mode scan is shown in fig 4. The mixed-mode scan architecture has three main components: The multiple Serial Scan (MSS), RAS, and the test controller. The numerous serial scan part is denoted by p-serial, and the RAS part is represented by p-random. The p-serial part consists of multiple serial scan chains with inputs SI0, SI1, and SI2 and a MISR at the outputs to compact the test responses. The number of scan chains can vary depending upon the available number of test pins. The shift operation in p-serial is performed by using the scan enable cum scan clock signal SCK. The RAS part is denoted by p-random and implemented as PRAS architecture. The row

address shift register and column driver are used for writing test data. The test controller generates control signals to drive the bit and bit-bar lines using the column driver based on the column address. The Sense Amplifier and MISR block are used to read and compact the test response data. The MISR for p-serial and p-random are connected serially with the controller to shift the test response signature via the scan I/O port. The two input signals, test-mode0 and test-mode1, connected to the test controller are used to operate the circuit between functional mode and the test mode and exercise the test.

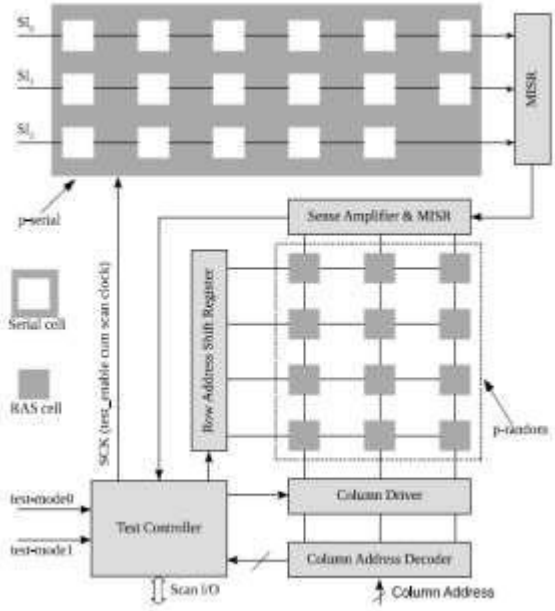

Fig 4: Mixed mode scan design architecture

III. PROPOSED METHODOLOGY

Mixed Mode Scan Design: This section examines the use of this RAS discusses the flip-failure technique to perform mixed-mode checks. When a mixed output model, it is the case that a part of flip-flops is used for framing sequential scan while the remaining flip-flops form RAS engineering. Both the sequential scan test engineering, as well as RAS tests, are developed simultaneously. Flops integrated into sequential scan designs are replaced by a flip-flop for sequential work when performing this composite output. The flip-tumbles integrated into RAS engineering are replaced by a RAS cell. In the blended model, examine the structure; the clock should be maintained high throughout the test mode to carry out RAS cell read/compose activities. The sequential output component cannot be performed in parallel with RAS by using the conventional serial scan cells. The proposed scanner cell addresses this problem by using the test control movement as a moderate recurrence clock that allows simultaneously in both configurations in parallel.

The proposed scan design eliminates the need for two separate scan cell libraries to implement

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the serial scan and RAS parts. It provides a standard scan cell that can be used both as a serial scan cell and a RAS cell. Schematic design of area and performance efficient, progressive random access scans cell is shown in fig 5 and serial part respectively. The first step in mixed mode scan architecture implementation is the segregation of all the flip flops into two groups. One group of the flip-flops is assigned to the serial port and the flip-flops from the second group go into the RAS part.

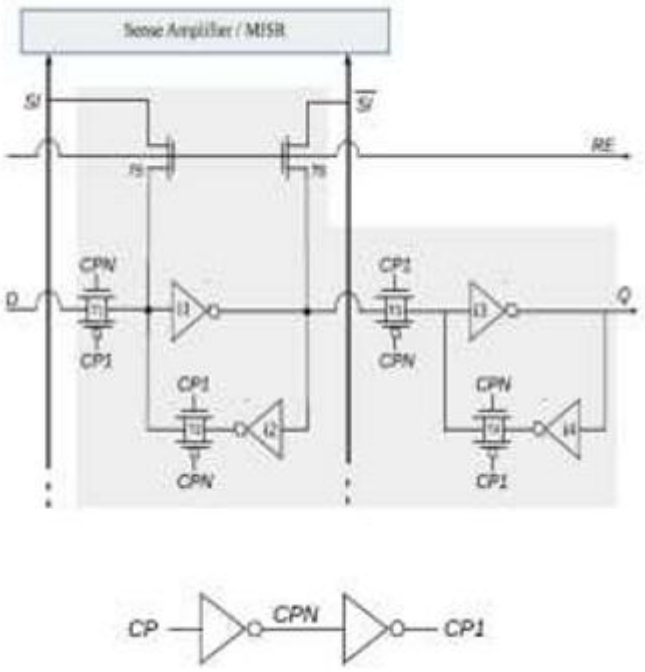

Fig5: Random Access Scan (PRAS) Cell

For Proposed Work, we can modify the architecture by removing the serial data processing unit, and we use the RAS cells for serial communication. The modified mixed mode scan design architecture is shown in fig 6.

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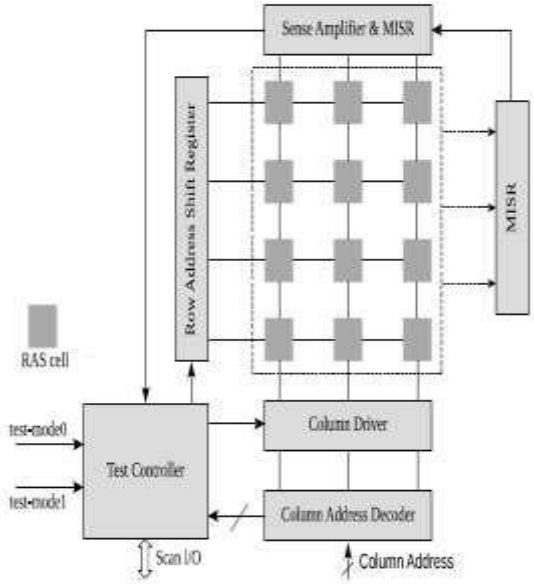

Fig6: Proposed Mixed mode scan design architecture

The segregation of scan cells among serial ports and the RAS part is very crucial for test time, test data volume, test power dissipation, and area overhead. For the current work, we have used a simple criterion based on test pattern care bits. The scan cells for which most of the patterns are specified with care bits are included in the serial scan part. Whereas those scan cells for which most of the test patterns have unspecified or don't care bits are included in the RAS part.

The functionality of the circuit is controlled by the two test mode control signals, test-mode0 and test-mode1. Depending upon the states of the test control signals, the course can operate in four modes. When both signs are 0, the circuit operates in normal functional mode. The remaining three states are mixed-mode (01), p-random mode (10), and p- serial-mode (11). The test process starts with mixed-mode with p-serial and p-random loading/unloading the test stimuli/response concurrently. The shift operation in p serial, synthesized using the read/write operation in p-random, is carried out in two steps. First, the row enables signal is asserted to read the existing state of the RAS cells. Note that the read/write operation in RAS corresponds to the loading or unloading of test stimuli/response.

IV. RESULTS AND EVALUATION

The total designs are done and implemented in Xilinx ISE 14.7 with Verilog HDL coding.

Table I: Comparison of Existing and Proposed method.

Parameters	Mixed mode proposed	Mixed mode extension
Area	132 LUT's	89 LUT's

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Delay	4.905 ns	4.805ns

V. CONCLUSION

The area-efficient scan chain design is suggested to overcome the performance issues because of the critical path and the high use of multiplexers in design. It replaces random scan architectures for mix mode designs. The proposed method for mixed-mode is suitable for both traditional and test processes. Additionally, the proposed scan flip-flop could be used as serial scan cells and a RAS cell in testing with mixed modes. A mixed-mode scan model, which is based on the proposed flip-flop for scanning, shows a promising reduction in the length of the interconnect wire and test data volume and time to test.

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