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DESIGN AND IMPLEMENTATION OF FIR FILTER BASED ON COMPRESSORS

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ABSTRACT:

In this paper, we propose four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. Multiplication is basic functioning arithmetic operations. Multiplication based operations such as multiply and Accumulate unit (MAC), convolution, Fast Fourier Transform (FFT), filtering (FIR) are widely used in signal processing applications. As, multiplication dominates The execution time of DSP systems, there is need to develop high speed multipliers. In the approximate mode, these dual quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of these compressors in a 32-bit Dadda multiplier for FIR Filter are evaluated using Verilog HDL and simulated and synthesized using Xilinx 14.5. Comparing their parameters with those of the existing Wallace tree multiplier designed using 4:2 and 5:2 compressors. The results of comparison indicate the lower delay and power consumption in the approximate mode.

Keywords: Dadda, HDL, FFT, FIR, MAC.

1. INTRODUCTION

We propose four 4:2 compressors, which have the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these dual-quality compressors provide higher speeds and lower power consumptions at the cost of lower accuracy. Each of these compressors has its own level of accuracy in the approximate mode as well as different delays and power dissipations in the approximate and exact modes. Using these compressors in the structures of parallel multipliers provides configurable multipliers whose accuracies (as well as their powers and speeds) may change dynamically during the runtime. The efficiencies of

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these compressors in a 32-bit Dadda multiplier are evaluated in a 45-nm standard CMOS technology by comparing their parameters with those of the state-of-the-art approximate multipliers. The results of comparison indicate, on average, 46% and 68% lower delay and power consumption in the approximate mode. Also, the effectiveness of these compressors is assessed in some image processing applications. The proposed architecture of this paper analysis the logic size, area and power consumption

VLSI:

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors. VLSI stands for "Very Large Scale Integration". This is the field which involves packing more and more logic devices into smaller and smaller areas. Thanks to VLSI, circuits that would have taken board full of space can now be put into a small space few millimeters across! This has opened up a big opportunity to do things that were not possible before. VLSI has been around for a long time, there is nothing new about it, but as a side effect of advances in the world of computers, there has been a dramatic proliferation of tools that can be used to design VLSI circuits. Alongside, obeying Moore's law, the capability of an IC has increased exponentially over the years, in terms of computation power, utilization of available area, yield. The combined effect of these two advances is that people can now put diverse functionality into the IC's, opening up new frontiers. Examples are embedded systems, where intelligent devices are put inside everyday objects, and ubiquitous computing where small computing devices proliferate to such an extent that even the shoes you wear may actually do something useful like monitoring your heartbeats. Verilog was developed at a time when designers were looking for tools to combine different levels of simulation. In the early 1980s, there were switch-

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level simulators, gate-level simulators, functional simulators (often written ad-hoc in software) and no simple means to combine them. Further, the more-widespread, traditional programming languages themselves were/are essentially sequential and thus "semantically challenged" when modeling the concurrency of digital circuitry.Verilog was created by Phil Moore in 1983-4 at Gateway Design Automation and the first simulator was written a year later. It borrowed much from the existing languages of the time: the concurrency aspects may be seen in both Modula and (earlier) Simulate; the syntax is deliberately close to that of C; and the methods for combining different levels of abstraction owe much to Hilo.

EXISTING SYSTEM:

While there are many works in designing approximate multipliers, the research efforts on accuracy configurable approximate multipliers are limited. In this section, we review some of these works. In [10], a static segment method (SSM)is presented, which performs the multiplication operation on an m-bit segment starting from the leading 1 bit of the input operands where m is equal to or greater than n/2.Hence, an m×m multiplier consumes much less energy than an n×n multiplier. Also, a dynamic range unbiased multiplier (DRUM) multiplier, which selects a nm-bit segment, starting from the leading 1 bit of the input operands, and sets the least significant bit of the truncated values to “1,” has been proposed. In this structure, the truncated values are multiplied and shifted to the left to generate the final output. Although, by exploiting smaller values form, the structure provides higher accuracy designs than those, its approach requires utilizing extra complex circuitry.A bio inspired approximate multiplier, called broken array multiplier, has been proposed. In this structure, some carry save adder cells, in both vertical and horizontal directions during the summation of the partial products, have been omitted to save the power and area and reduce the delay. Two approximate 4:2

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compressors have been proposed and utilized in Dadda multiplier. The proposed compressors only operated in the approximate mode. By modifying the Karnaugh map of a 2×2 multiplier (omitting one term in the Karnaugh map), an approximate 2×2 multiplier with a simpler structure has been proposed. This block may be usedfor constructing larger multipliers. Also, in this paper, an error detection and correction (EDC) circuit has been proposed. An inaccurate multiplier design strategy based on redesigning the multiplier into two multiplication and non-multiplication parts was introduced. The multiplication part was constructed based on the conventional multipliers while then on-multiplication part was implemented in an approximate structure with a specified value of error. It should be noted that both of the approaches presented suffer from high relative errors.

A high accuracy approximate 4×4 Wallace tree multiplier was proposed. This multiplier employed a 4:2 approximate counter leading to delay and power reductions of the partial product stage of the 4×4 Wallace tree. In this paper, the proposed small multiplier was used to form larger multipliers. Due to the array structure of this approximate multiplier, its delay was large. In addition, an EDC unit was suggested to be used at the output of the approximate 4 ×4 Wallace tree. The unit generated the exact output in the case of the exact operating mode. By proposing an approximate adder with a small carry propagation delay, the partial product reduction stage was sped up. In this paper, an OR-gate-based error reduction unit was also proposed. A rounding based approximate multiplier (ROBA) has been proposed that round the input operands into the nearest exponent of two. This way the multiplication operation became simpler. It should be noticed that the error recovery unit increases the power consumption and delay of the

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multiplier. This implies that accuracy configurable multipliers would have large delay and power overheads.

2. LITERATURE SURVEY:

Khaing Yin Kyaw et al. [1] in their proposed an algorithmic approach of multiplier design where the input to the multiplier is divided in two parts (i) non-multiplication part to give the lower order bits of the final output and (ii) multiplication part to generate the higher order bits of the product. The Least Significant Bit (LSB) related part will only check for 1 in the input pattern after which it will take 1 as output otherwise 0. The whole operation can be implemented with any number of inputs with no hard and fast rule that these parts should be equal. The choice of two parts depends upon the resulted error acceptance threshold values. In their design they conclude that with more no of input bits this approach can give better results. Due to less logic complexity both power and area is reduced.

Parag Kulkarni et al. [2] proposes an approach of architecture modification of multiplier block where inaccuracy is introduced only when all the input bits are 1. From the analysis of truth table and simplification they conclude that if the output in the case of all 1's in the input is truncated then the logic implementation of multiplier will be using less numbers of gates for their operation. With this approach for 2x2 multiplier block approximation uses only three output lines instead of four. This will results into forming a multiplication block with no XOR gates. Also the critical path delay in this case will be less by one gate delay compared to conventional structure. The error is present with a magnitude of 2. Larger multipliers are built by using the inaccurate 2x2 block to produce partial products and then adding the shifted partial products. Although error probability is increased with this approach the mean error is more or less almost same with input bit width increase

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Vaibhav Gupta et al. [4] proposed an inaccurate or rather say approximate adder structure which can be used in many application including multiplication. Their proposed design contains schematic level of changes with main goal of switching power reduction with less number of transistor use. Upon reviewing the full adder output combinations they conclude total four approximate full adder circuit with different error in sum and carry bit. With all these four one approximation with the observation of sum is actually inverted version of carry output in six cases out of eight contains the less amount of error.

Cong Liu et al. [5] described a structure combining approximation and error correction. In their approach they preprocessed the input data based on the interchangeability of bits with the same weights in different addends to form propagate and generate signals which fed into parallel adders to reduce the delay. The preprocessed input data processing performs on interchangeability of same weight input bits. Here instead of carry propagated to the higher bit which in turn increased the delay, an error signal is produced in parallel. These error signals are preventing the propagation of carry signal. These error signals are produced at each stages of operation can be added after each stage. This error signals are accumulated after each stage. To reduce the error, this accumulated error vector is added to the adder tree output using a conventional adder to produce final stage output. This configurable error recovery that can produce more accurate results.

Georgios Zervakis et al. [10] explored a new space for applying approximation in multiplier circuit. In their approach they applied perforation in the partial product generation stage. The partial product perforation technique omits the generation of some successive partial products starting from a specific position. A perforated partial product is not inserted in the

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accumulation tree, and hence some full adders can be eliminated. This approach is different with the truncation method where removing circuit elements is done on the accumulation of partial product stage. The proposed technique omits a number of partial products enabling high area and power savings while retaining high accuracy.

3. PROPOSED SYSTEM:

We present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig, in the exact operating mode, tri-state buffers are utilized to disconnect the outputs of the approximate part from the primary outputs.

The supplementary part of this structure is an exact4:2 compressor. The overall structure of the proposed structure is shown in Fig. 4(b). In the exact operating mode, thedelay of this structure is about the same as that of the exact4:2 compressor.

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2) Structure 2 (DQ4:2C2): In the first structure, while ignoring Cout simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output Cout is generated by connecting it directly to the input x3 in the approximate part. Fig. 5 shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1,namely, 62.5%, its relative error is lower.

3) Structure3(DQ4:2C3): The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. 6(a). In this structure, the accuracy of output sum' is increased. Similar to DQ4:2C1, the approximate part of this structure does not support output Cout. The error rate of this structure, however, is reduced to 50%.

4) Structure4(DQ4:2C4):In this structure, we improve the accuracy of the output carry' compared with that of DQ4:2C3at the cost of larger delay and power consumption where the error rate is reduced to 31.25%. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown. The supplementary part is indicated by reddashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line.

In this paper, we present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the

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approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

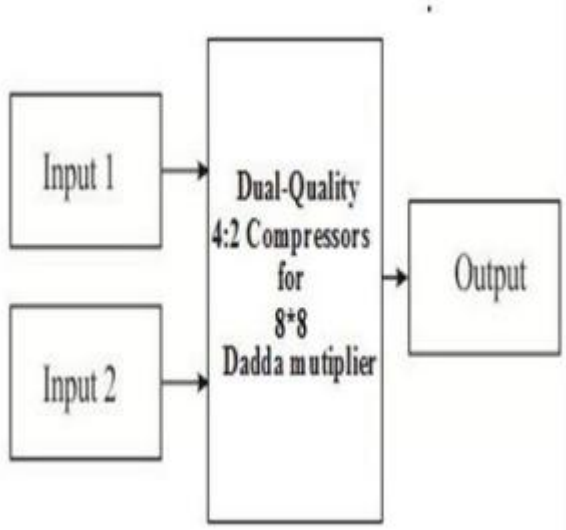

Figure 1: Block diagram of proposed system

4. RESULTS EXPLANATION

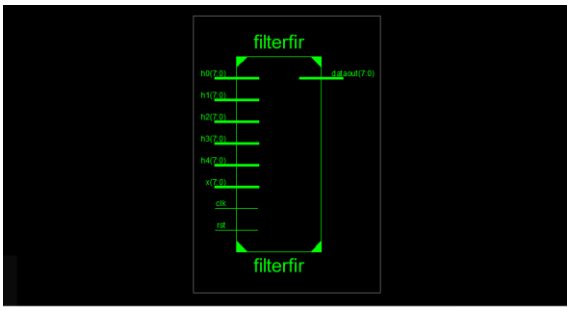

Fig.2. Circuit model.

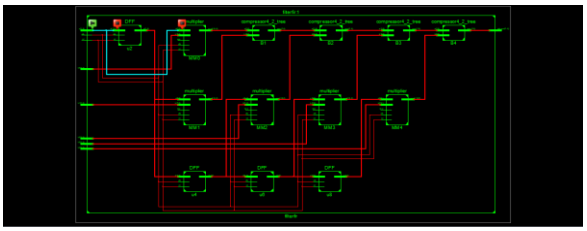

Fig.3. RTL diagram.

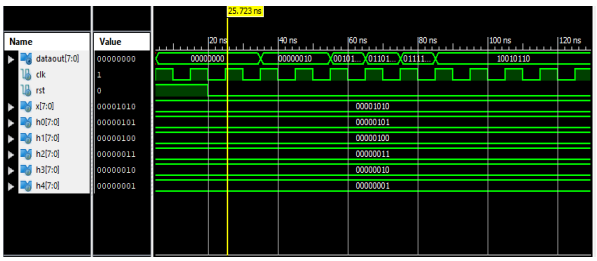

Fig.4. Simulation results.

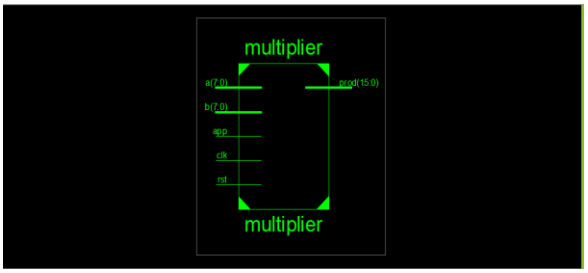

Fig.5. Multiplier circuit.

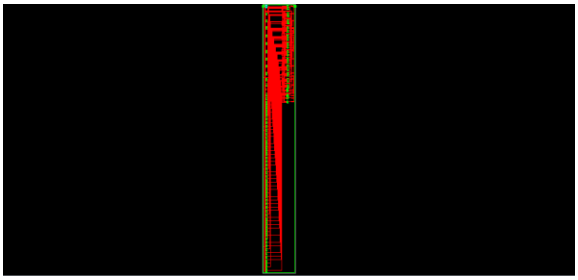

Fig.5. Model of internal circuit.

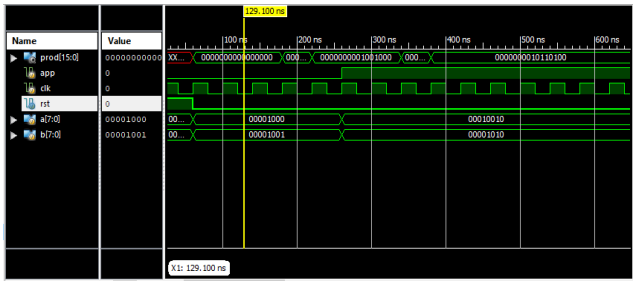

Fig.6. Simulation results.

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Selected Device : 6vcx75tff484-2


Slice Logic Utilization:
 Number of Slice Registers:             284  out of  93120     0%
 Number of Slice LUTs:                  223  out of  46560     0%
    Number used as Logic:               223  out of  46560     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    290
   Number with an unused Flip Flop:       6  out of    290     2%
   Number with an unused LUT:            67  out of    290    23%
   Number of fully used LUT-FF pairs:   217  out of    290    74%
   Number of unique control sets:        10

IO Utilization:
 Number of IOs:                         35
 Number of bonded IOBs:                 35  out of    240    14%
    IOB Flip Flops/Latches:              1

Specific Feature Utilization:
 Number of BUFG/BUFGCTRL/BUFHCEs:        1  out of    104     0%
```

Fig.7. power summary.

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Timing Summary:
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Speed Grade: -2

   Minimum period: 1.095ns (Maximum Frequency: 913.159MHz)
   Minimum input arrival time before clock: 1.400ns
   Maximum output required time after clock: 1.286ns
   Maximum combinational path delay: 0.894ns
```

Fig.8. Time summary.

5. CONCLUSION:

In this project, we have a tendency to propose fourDQ4:2Cs that had the flexibility of change between the exact and approximate operating modes. Within the approximate mode, these compressors provided higher speeds and lower power consumptions at the cost of lower accuracy. Every of those compressors had its own level of accuracy within the approximate mode moreover as different delays and powers within the approximate and exact modes. The proposed compressors are implemented on structure of a 8-bit Dadda multiplier, to estimate the performance of the proposed compressors. Our studies disclosed that for the 8-bit multiplication, the projected compressors have lower delay and power consumption within the approximate mode compared with those of existing compressors.

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