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DESIGN OF BUILT IN SELF TEST EMBEDDED MASTER SLAVE COMMUNICATION USING I2C PROTOCOL

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Abstract— The I2 C (Inter-Integrated Circuit) protocol is used to attach two devices for communicating with each other in a fast way excluding data losses. With the fast development of Integrated Circuits (ICs) technology, the complication of the circuits has also raised. Therefore, the complexity of the circuit requires self-testability in hardware to palliate the product failure. Built-in-self-test (BIST) is such a technique which can meet the necessity of self-testability with an effective solution over pricy circuit testing system. This paper represents designing and implementation of Inter-Integrated Circuit (I2 C) protocol with self-testing ability. The need of programming for setting up a network with two devices is no longer needed in this proposed system. In order to attain compact, stable and reliable data transmission, the I2 C is designed with Verilog HDL language and synthesized.

1. INTRODUCTION

The I2C (Inter-Integrated Circuit) is a two-wire bus, which is low to medium speed, communication bus (a path for electronic signals) developed by Philips Semiconductors in the early 1980s.The I2C was develop or created to reduce the manufacturing costs of electronic products.I2C is an bidirectional serial bus, which gives effective data communication between two devices. The actual or physical I2C bus consists of just two wires, which are SCL and SDA. The SCL is a serial clock line; it is used to synchronize the whole data transfers over the I2C bus. Besides that, SDA is the serial data line; it is used to carries the data. The SCL and SDA lines are connected to all devices on the I2C bus. Fig.1 shows the Format of I2C bus protocol bus.

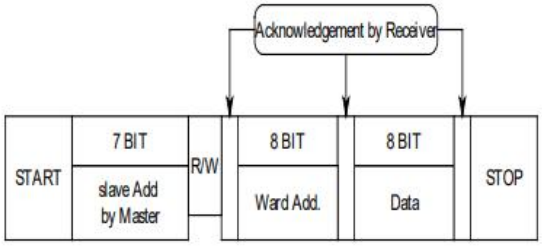

Fig.1: Format of I2C Protocol Bus

The Inter-Integrated Circuit commonly termed as I2C is a protocol that is mend for attaching two devices for communicating with one another with high speed without any data losses. Since Technologies of Integrated Circuits (ICs) are developing with high speed, the circuits are getting more complicated. In order to overcome the complexity of the circuits, self-testing is must in hardware to in order to reduce frequency of the product failure. This requirement is fulfilled by a technique called Built-in-self-test (BIST) with an effective solution over high cost circuit testing system. Verilog is used to understand, analyze and implement the READ and WRITE operation. The design is verified and synthesized for FPGA implementation using Xilinx ISE tools.

2. DESINGNED ARCHITECTURE

The illustrating square configuration of the finished correspondence assistants among I2C and APB is appeared in Fig. 2. The Structure contains two basic pieces, i.e. I2C Slave and APB Master. I2C Slave takes the information from I2C Master in isolated course of action and offers it to APB Master. This APB Master likewise passes on this information to APB Slave in APB Protocol. In this manner a correspondence between I2C Master and APB Slave is finished.

A. Write Operation

1) Whenever I2C Master needs to visit with APB Slave it would be done by frameworks for I2CSlave.
2) I2C Slave will affirm Data Valid and Address Valid signs.
3) Seeing these banners high, masterminded APB Master considers the memory for its responsiveness and begins APB shape state machine.
4) I2C sends four bits of 8-bit information serially to be shaped on APB Memory at four unfaltering spaces.
5) After trade of every byte APB Master keeps a mind tally whether each and every one of the four memory territories are vivified sensibly.
As soon as the information at APB Master is restored it traded the same 32-bit information to APBSlave.

B. Read Operation

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Here again when I2C need to investigate information from the APB slave, Correspondence will occur through APB master to I2C slave to I2C master APB Salve will send a banner to APB Master empowering that the information is available to be examined. APB Salve by then transmits the data to APB Master where it is secured in the internal memory to be brought by I2C Slave at time explanation behindtime

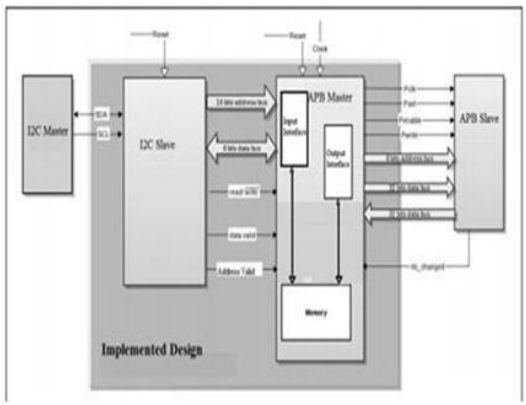

Fig.2: Communication Bridge

C. AHB APB Interface

Focus AHB to APB is an AHB slave and AMBA APB Master that gives an interface (associate) between the fast AHB space and the low-control APB territory. The Core AHB to APB interfaces with Core AHB/Core AHB Lite through the AHB interface, orCore APB through the APBinterface.

D. Key Features

1) Bridges between Advanced Microcontroller Bus Architecture (AMBA) Advanced High-Performance Bus (AHB) and Advanced Peripheral Bus(APB).

2) Automatic relationship with Core AHB/Core AHB Lite and Core APB in Smart Design.

3) AMBA APBagreeable.

E. Maintained Interfaces

Center AHB to APB supports an AHB or AHB-Lite slave interface related with an AHB or AHB-Lite reflected slave interface (for example, Core AHB or Core AHB Lite) and likewise an AMBA APB pro interface that interfaces with an AMBA APB reflected pro interface (for example, CoreAPB)

F. BlockDiagram

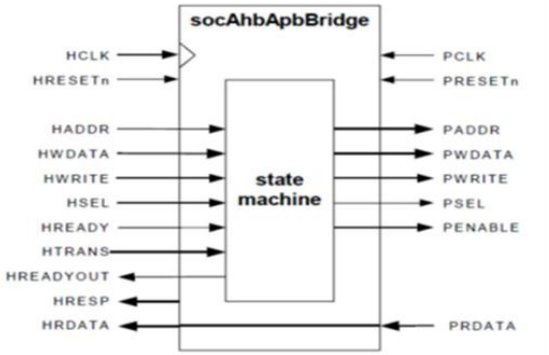

Fig.3: AHB and APB Bridge

G. Description

The I2C-APB Bridge is used make a translation of AHB signs to APB signals. The I2C-APB Bridge is moreover used to isolate the tip top AHB (system transport) from the slower APB (Peripheral Bus). The I2C-APB Bridge is an AHB slave part which recognizes trades concentrating on an APB periphery, unravels the address, and gives an APB, periphery transport, trade to the concentrated-on periphery or memory. The I2C-APB Bridge can decipher up to sixteen APB peripherals. On create trades, the I2C-APB Bridge gives the form control (PWRITE), select (PSELx), and address (PADDR) and data (PWDATA) to the concentrated-on periphery or memory. On read trades, the I2C-APB Bridge multiplexes the concentrated-on periphery's data (PRDATA_device) to the AHB HRDATA with the most ideal arranging. The I2C-APB Bridge furthermore reestablishes the HREADYOUT movement back to the AHB pro to show that the IPC-APB Bridge has completed the APB trade and the data isreadied.

H. Interfacing APB toAHB

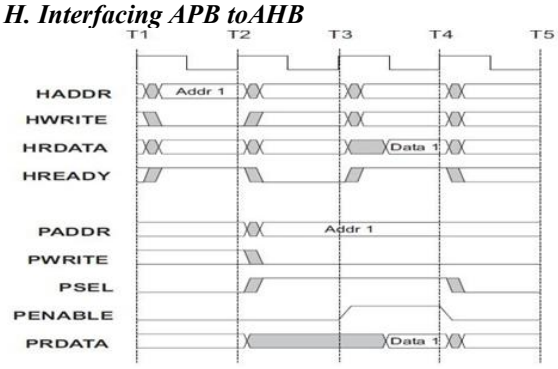

Fig.4: Interface APB to AHB

The exchange starts on the AHB at time T1 and the address is investigated by the APB interface at T2. In case the trade is for the periphery exchange then this address is conveyed and the best possible periphery select flag is created. This first cycle on the periphery exchange is known as the SETUP

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cycle, this is trailed by the ENABLE cycle, when the PENABLE banner is certified. In the midst of the ENABLE cycle the periphery must give the read data. Routinely it will be possible to course this read data particularly back to the AHB, where the transport ace exchange can test it on the rising edge of the time toward the complete of the ENABLE cycle, which is at time T4. In high clock repeat systems, it may wind up essential for the expansion to select the read data toward the complete of the ENABLE cycle and thereafter for the framework to drive this back to the AHB transport expert in the going with cycle. Regardless of the way that this will require an extra sit tight state for periphery exchanges read trades, it allows the AHB to continue running at a higher clock repeat, accordingly achieving a general change in system execution. A burst of read moves is showed up in Figure. All read trades require a singular hold up state.

I. WriteTransfer

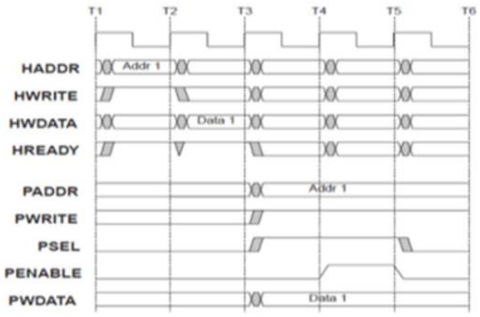

Fig.5: Write Transfer

The transfers begin on the AHB at time T1 and the address is examined by the APB interface at T2. If the trade is for the periphery exchange then this address is imparted and the correct periphery select flag is delivered. This first cycle on the periphery exchange is known as the SETUP cycle, this is trailed by the ENABLE cycle, when the PENABLE banner is insisted. In the midst of the ENABLE cycle the periphery must give the read data. Consistently it will be possible to course this read data particularly back to the AHB, where the exchange Master can test it on the rising edge of the time toward the complete of the ENABLE cycle, which is at time T4. In high clock repeat systems, it may wind up imperative for the expansion to enlist the read data toward the complete of the ENABLE cycle and thereafter for the framework to drive this back to the AHB move transport ace in the going with cycle. In spite of the way that this will require an extra sit tight state for periphery exchange read trades, it allows the AHB to continue running at a higher clock repeat, consequently realizing a general change in structure execution. A burst of readmoves is showed up in Figure. All read trades require a singular hold upstate.

3. RESULTS

Circuit Schematic Fig. 6 & Fig. 7 shows the pin diagram and top level diagram of the I2 C with BIST capability circuit respectively.

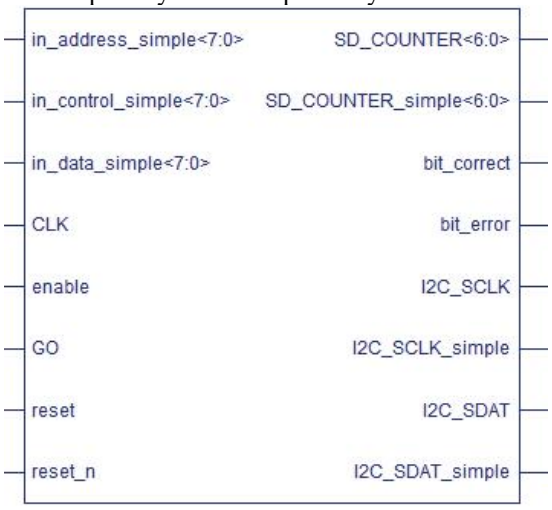

Fig. 6. Pin Diagram of I2 C

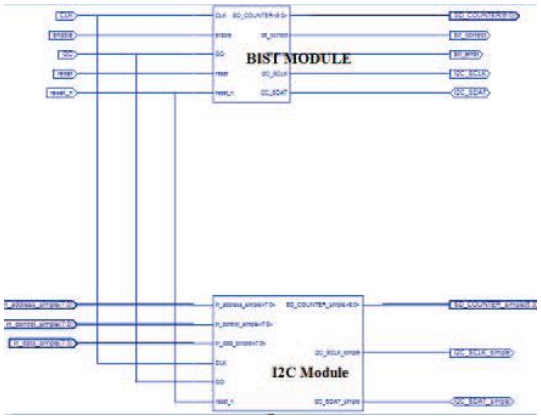

Fig. 7. Top level schematics of I2 C with BIST capability.

In Fig. 8, the top level schematic of BIST module is shown. As described earlier, BIST module consists of three LFSRs and one comparator is depicted in the Fig. 8.

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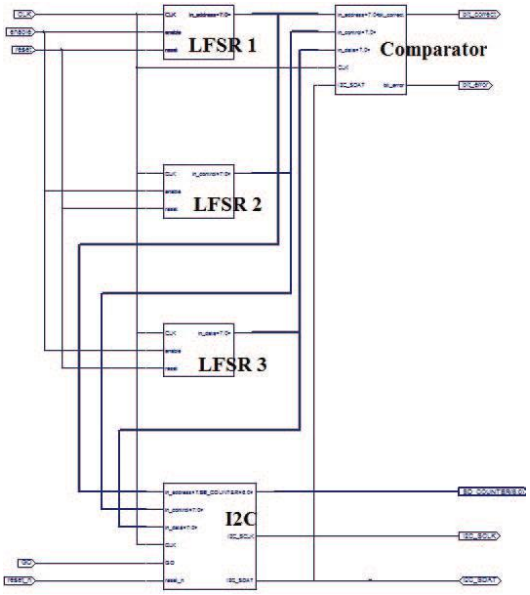

Fig.8. Top level schematics of BIST Module

The timing diagram achieved from Test bencher showed that the received data in the receiver. Then the design is tested in the Xilinx FPGA where it also gave the correct output. The 8 bits of outputs are converted here into 2-digits Hexadecimal numbers.

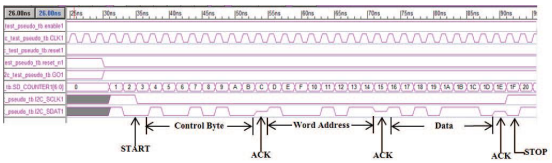

Fig. 9. BIST mode Output.

Fig. 9 shows the timing diagram of the I2 C output in the BIST mode. Three Random Pattern Generators generate random bits for the 8-bit control byte, 8-bit word address and 8-bit data. When the "reset_n" is low and "GO" is high then the control bytes, word address and data bits are passed depending on the "ACK" from the slave. When the "START" bit is passed, then the control byte start passing through the I2C bus. After that, an acknowledgement (ACK) is given by the slave. The next 8-bit is the word address or the memory. Address which is passed. Then, an "ACK" from the slave is given and 8-bit data is passed. Then, the "ACK" is given from slave and at last, the stop bit ends the operation. The process continues. And in this process, the efficiency and bit error rate of the I2 C can be tested.

CONCLUSION

The AHB-IIC module is thus designed and checked for correct outputs. Thus the designed module combines the advantages of both AHB and IIC and promises a high performance, speed matching module which will make the communication between the processor and an IC more efficient by reducing the area and external peripherals. The flexibility of the communication is also increased because of the two cycle phase concept of the AHB thus giving a highly advantageous outcome. The functional coverage is obtained to be 100%. The synthesis report in terms of speed and frequency is inferred in the table below,

PARAMETERS	AHB	IIC
Speed	20Mbps	100Kbps
Frequency	10MHz	50KHz

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