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DESIGNING OF COMBINATIONAL LOGIC CIRCUITS BASED ON REVERSIBLE DECODER

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***Abstract*—** Reversible logic is the emerging field for research in present era. The aim of this paper is to realize different types of combinational circuits like full-adder, full-subtractor, multiplexer and comparator using reversible decoder circuit with minimum quantum cost. Reversible decoder is designed using Fredkin gates with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and many more. Reversible logic is defined as the logic in which the number output lines are equal to the number of input lines i.e., the n-input and k-output Boolean function F(X1, X2, X3,…, Xn) (referred to as (n, k) function) is said to be reversible if and only if (i) n is equal to k and (ii) each input pattern is mapped uniquely to output pattern. The gate must run forward and backward that is the inputs can also be retrieved from outputs. When the device obeys these two conditions then the second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back are not allowed in Logical Reversibility. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI Etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption. The comparative study in terms of garbage outputs, Quantum Cost, numbers of gates are also presented. The Circuit has been implemented and simulated using Xilinx software.

I. INTRODUCTION

In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible Decoder for designing Combinational circuits power consumption is reduced to an optimum when compared to conventional decoder based combinational circuits. Reversible Logic finds its own application in Quantum computing, Nano-technology, optical computing, computer graphics and low Power VLSI. Ralf Launders [1] told that heat dissipation in circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the process. He introduced that losing of a single bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant and T is Temperature. The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits which imply propagation delay also. Later in 1973 C. H. Bennett described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit. As the transistors get smaller, the power density of those transistors remains constant so that the used power is proportional with area and this law is called as Dennard's Scaling or MOSFET scaling. Dennard's scaling failed mainly due to the fact that supply voltage remained constant but the power densities subsequently increase on the chip. Therefore, a major quantity of on-chip resources has to stay in power-gated situation, so as to avoid thermal emergencies. In this scenario, transistor and voltage scaling don't seem to be in line with one another. In recent years, reversibility assumes a major role when computations with least energy dissipation are examined. Reversible technology is used in various areas such as low power CMOS design, Nano-Technology, Quantum & Optical computing, DSP, etc. It is used for reducing power consumption and loss of data. In reversible technology there is no information loss at reversible logic so zero energy consumption takes place. It will help to avoid heat generation. In Digital Electronics, for design of combinational and sequential circuits various techniques are used. Design of a combinational circuit using binary decoder is one of them.

II. EXISTING METHOD

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder whose Quantum Costas less than the previous design. Replacing Fredkin gates for designing 2×4 decoder reversible gates like peres gate, TR gate, NOT gate and CNOT gate are used as shown in figure9. The whole design is done

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using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 Fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder.

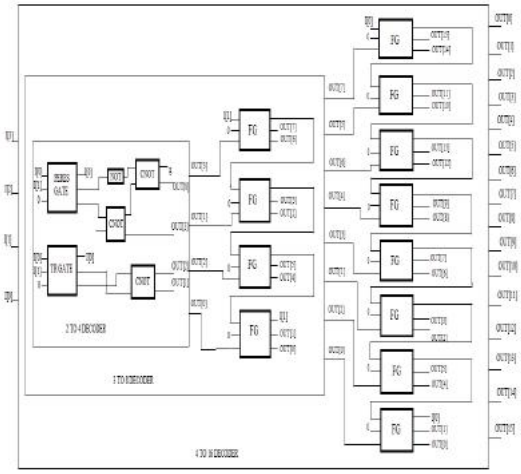

Figure-1: Existing System

III. PROPOSED SYSTEM

Different Reversible Decoder circuits like 2×4, 3×8, 4×16 are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinational circuits like comparator adder, subtractor, multiplexers etc., are designed using these decoders. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation.

3.1 Reversible logic gate:

It is not apart advice us to dispose the results against the inputs but also advise us to incompatibly balance the inputs from the results.

3.2 Garbage output:

It is also associate to the representation of results which are not used in the synthesis of provided activity. In assertive covering these incline compulsory to accomplish reversibility.

Constant input value+ Input value = Garbage value + Output value

3.3 Quantum cost:

The quantum cost of the design is less figure of 2*2 integrated gates to exhibit the design observance the results constant.[5]It is accredit to the cost of the design in the details of the part of a primary gate.

3.4 Flexibility:

Its indicate the collectivity of a reversible logic gates which accomplishing many activities.

3.5 GateLevel:

This associate the fraction of objectives in the design which is useful to conceive the provided connection.

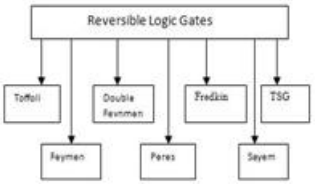

Figure-2: Different types of logic gates

3.6 Feynmen Reversible Logicgate

In this gate input and output is given by input [P, Q] and output [L,M]. So where the output is provided as L=P and M=P⊕Q.

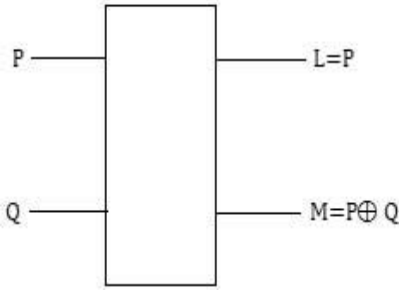

Figure-3: Feynman Gate

a) Double Feynmen Reversible Logic gate

In this gate input and the output is given by input [p, q, and r] and output [l, m, n]. Where the output is provided as l=p, m=p⊕q and n=p⊕r.

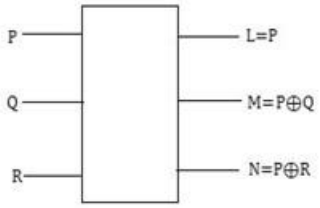

Figure-4: Double Feynman Gate

b) Toffoli Reversible Logic gate

In this gate, input and output is given by input [P, Q and R] and output [L,M,N]. Where the Output is provided as L=P, M=Q and N=PQ⊕R. Its quantum cost is 5.

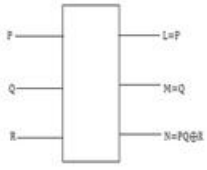

Figure-5: Toffoli Gate

c) Fredkin Reversible Logicgate

In this gate input and output is given by input [P,Q and R] and output [L,M,N]. Where the output response is L=P, M=PQ⊕PR, N=P'R⊕PQ.**[8]**

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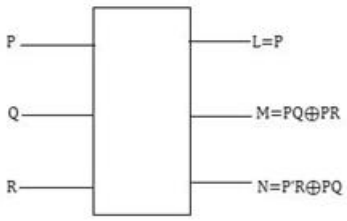

Figure-6: Fredkin Gate

d) Peres Reversible Logic gate

In this gate input and output is given by input[P,Q,R] and output[L,M,N] and its result is L=P, M=P⊕Q, N=PQ⊕R. Its quantum cost is 4.

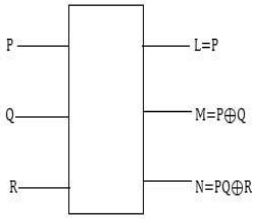

Figure-7: Peres Reversible Logic gate

e) TSG Reversible Logic gate

In this gate input and output is given by input[P,Q,R,S] and output[L,M,N,O]. This is performing is function single reversible full adder and operate by the Boolean function. So its provided output is L=P, M=P'Q⊕PR, N= P'Q⊕PR⊕S andO=PQ⊕P'R⊕S.

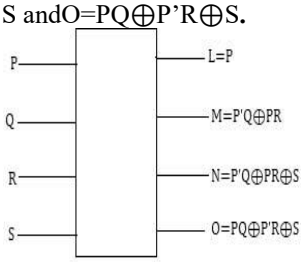

Figure-8: TSG Gate

IV. SIMULATION RESULTS

The entire simulation and result obtaining using test vectors are done with the help of Xilinx software. The concept of duplicating one output to two outputs using Feynman gate is introduced. The second input of Feynman gate was made to 0 which drives two splitted equivalent outputs.

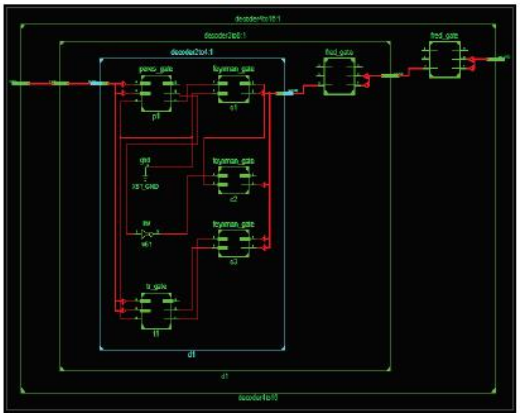

Figure-9: Reversible Deocder 4-16

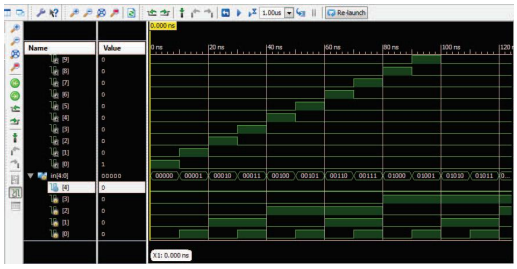

Figure-10: simulated output for 4 ×16 decoder

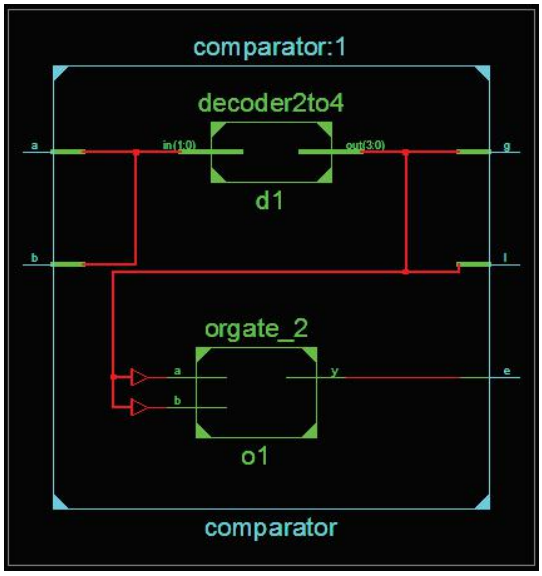

Figure-11: RTL Schematic of Binary Comparator

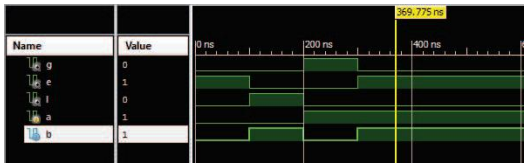

Figure-12: Simulated output for Binary Comparator

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The output lines g, l, e represents Greater, Lesser, Equal respectively. The a, b lines represents the inputs. If a<b then 'l' output becomes high. If a>b then 'g' output becomes high. If a=b then 'e' output becomes high.

FULL ADDER/ SUBTRACTOR

The concept of duplicating one output to two outputs using Feynman gate is introduced. The second input of Feynman gate was made to 0 which drives two splitted equivalent outputs.

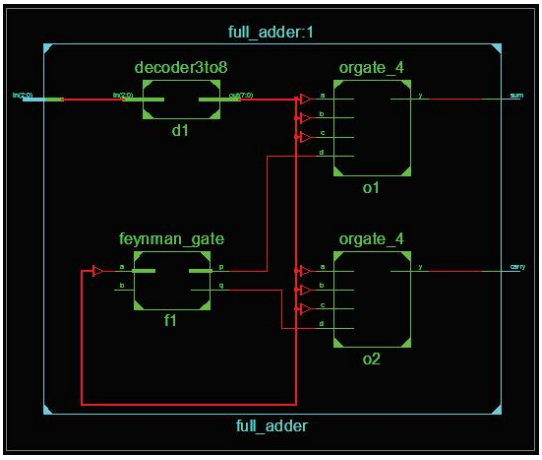

Figure-13: RTL Schematic of full adder

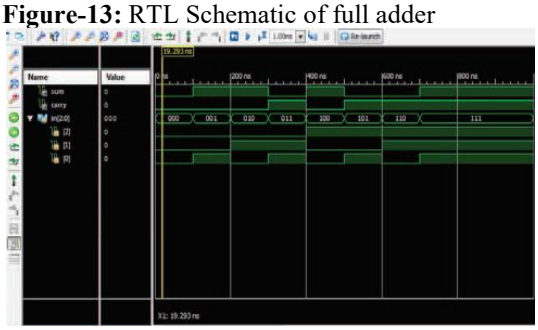

Figure-14: Simulated output for Full adder

For designing a full adder a 3 to 8 decoder and two four input OR gates are required. The min terms for SUM and CARRY are derived from output pattern of decoder. Similarly the full subtractor was also designed. The simulated output is shown in figure15. To design 4-bit full adder/subtractor circuit four full adders are required. The Cininput drives the first full adder. If Cin is given with low input 4-bit addition is performed and if Cin is given with high input the 4-bit subtraction in the form of 1's complement addition is performed.

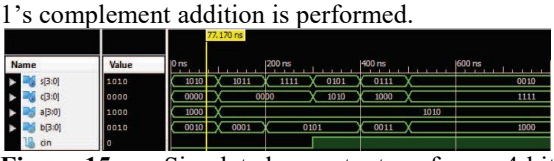

Figure-15: Simulated output for 4-bit adder/subtractor

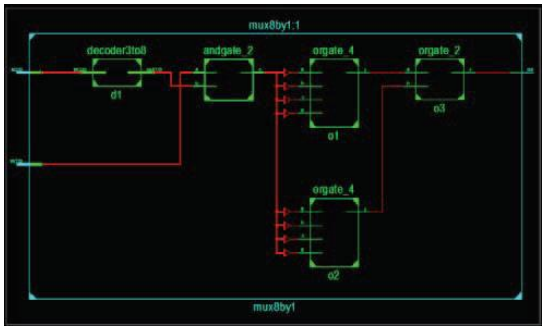

Figure-16: RTL Schematic of 8×1 multiplexer

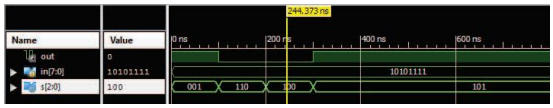

Figure-17: Simulated output of 8×1 multiplexer

To design a multiplexer using reversible decoder, reversible 2 input AND gates, 2 input OR gates are required. The 2 input AND Gate and OR gate are designed using Fredkin gate. By using these designed gates we can improve those gates to the required number of input gate. Each outputline from decoder is driven to 2 input AND gate along with multiplexer input. The outputs of all AND gates are made to drive to that particular input OR gate. The input binary integer values act as the selection lines. Similarly by using 4×16 decoder a 16×1 multiplexer is designed. The RTL Schematic and the simulated outputs of 16×1 multiplexer are shown in figure.

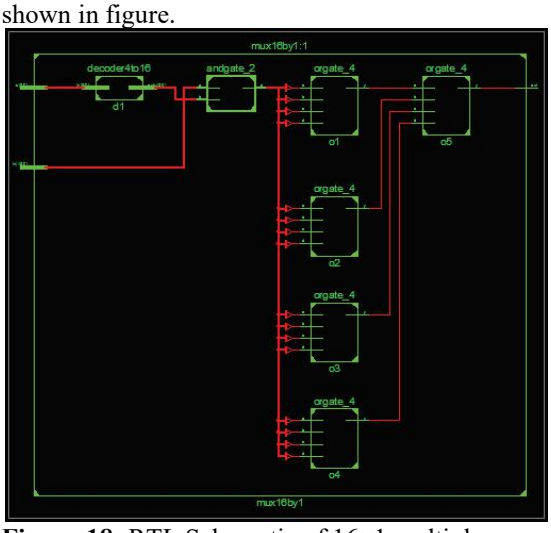

Figure-18: RTL Schematic of 16×1 multiplexer

V. CONCLUSION

In this paper, different combinational circuits like full adder, full subtractor, multiplexer, comparator circuits constructed using reversible decoder are designed. These circuits are designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the

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decoder circuit can be generalized. For example, a 3×8 decoder can be designed using a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 fredkin gates .The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance.

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