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DESING OF LOW POWER, HIGH PERFORMANCE 2-4 AND 4-16 MIXED-LOGIC LINE DECODERS

[1]SHAIK UZMA BEGUM, [2]J RAVISANKAR

[1] M tech student, Dept of ECE, *KRISHNAVENI ENGINEERING COLLEGE FOR WOMEN, NARASARAOPET, AP, India.*

[2]Professor, Dept of ECE, *KRISHNAVENI ENGINEERING COLLEGE FOR WOMEN, NARASARAOPET, AP, India.*

ABSTRACT:

This project presents a blended rationale plan technique for line decoders, joining transmission door rationale, pass transistor double esteem rationale and static CMOS. Two tale topologies are exhibited for the 2-4 decoders: a 14-transistor topology pointing on limiting transistor tally and power dispersal and a 15-transistor topology pointing on high power-defer execution. Both an ordinary and an altering decoder are executed for each situation, yielding an aggregate of four new plans. Besides, four new 4-16 decoders are planned, by utilizing blended rationale 2-4 predecoders joined with standard CMOS post-decoder. All proposed decoders have full swinging ability and lessened transistor tally contrasted with their ordinary CMOS partners.

Keywords: CMOS, 4-16, decoder, predecoder.

1. INTRODUCTION

Power management has became a major issue in the development of a digital system especially, in the portable devices in which enhancement of the battery life time and reducing the charging time are becoming a challenging issues day by day. The major issue is power dissipation. Technology scaling leads to Increase leakage current, which leads to increase in sub threshold leakage current. It is paramount that these high computational capabilities are placed in a low-potency, portable environment. Hence, a well orchestrated low energy design strategy must be in place. As the density of the integrated circuits and size of the chips and systems perpetuate to grow, it

becomes more and more arduous to provide adequate cooling for the systems. In integration to heat abstraction, there are economic and environmental issues for low power development. In the Amalgamated States, computer equipment accounts for about 2-3% of total power consumption. This figure is expected to increment as there is tremendous increase in household computer applications, Web phones, handheld computers, and internal terminals. These economic and environmental reasons have compelled the requisite for energy efficient computers. Static cmos circuits are used for the majority of logic gates in integrated circuits. They consist of complementary N-type metal-oxide-semiconductor (nMOS) pull down and P-type metal-oxide semiconductor (pMOS) pull up networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM). This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design.

2. LITERATURE SURVEY

Ritajit Majumdar In her article proposed a novel design of 2:4 decoders and

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has used it to build a 3:8 decoder. The quantum cost of an n: 2n decoder will reduce by use of their 2:4 decoder blocks. As for n input signals, the number of output signal will be 2n, still the increase in the number of gates will be linear in respect to the number of output signals. She also conclude that; use of other gates such as TR gate, Peres, or Toffoli gate the number of gates will be twice as high also the quantum cost will be nearly doubled. In the same manner the number of garbage outputs for all these gates also increases. Since every Fredkin gate has one garbage output; according to the author the design proposed in her paper cannot be optimized further by using the basic gates like Peres, Toffoli or TR gates. Landauer showed that the heat generated during computation is not due to the processing of bits, but due to the loss of information. Wiping of each bit of information causes a kTln2 amount of heat dissipation where k is the Boltzmann constant = 1.3805 _ 10^23 J/K and T is the temperature in absolute scale. While this heat may be negligible for a single wipe of information, in modern VLSI design, where many chips are arranged in small region and millions of instructions are processed per second, the information loss and consequently the heat generation is formidable.

EXISTING SYSTEM:

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary nMOS pulldown and pMOS pullup networks and present good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell based logic synthesis and design. Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single style design. Line decoders are fundamental

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circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of Boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including.

3. AN OVERVIEW OF PROPOSED SYSTEM

One of the exchanging terminals of the transmission door is raised to a voltage close to the negative supply voltage, a positive entryway source voltage (door to-deplete voltage) will happen at the N-channel MOSFET, and the transistor starts to lead, and the transmission door conducts. The voltage at one of the exchanging terminals of the transmission entryway is presently raised constantly up to the positive supply voltage potential, so the door source voltage is lessened (entryway deplete voltage) on the n-channel MOSFET, and this starts to kill. In the meantime, the p-channel MOSFET has a negative door source voltage (entryway to-deplete voltage) develops, whereby this transistor begins to direct and the transmission door switches. In this manner it is accomplished that the transmission door ignores the whole voltage run. The change obstruction of the transmission entryway fluctuates relying on the voltage to be changed, and compares to a superposition of the opposition bends of the two transistors.

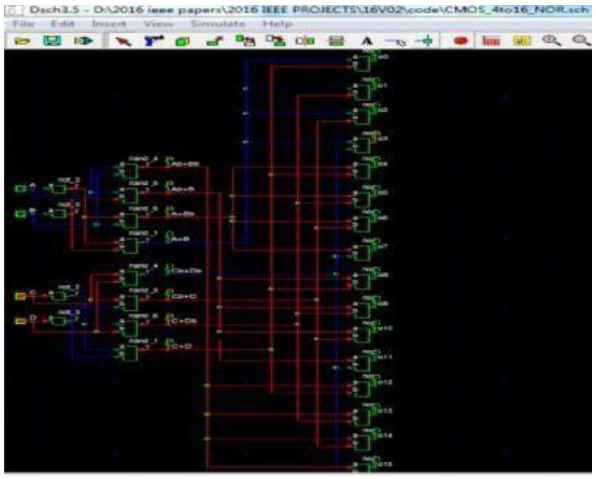

Fig. Schematic of 4to16 Decoder Using CMOS

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR gates. Decoders are high fan out circuits, where few inverters can be used by multiple gates, thus using the TGL/DVL gates can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, i.e the fact that they do not have balanced input loads. As shown in

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Fig. 2, we labeled the 2 gate inputs X and Y. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y inputs as the control signal and the propagate signal of the gate, respectively. This asymmetric feature gives a designer the flexibility to perform signal arrangement, i. e choosing which input is used as control and which as propagate signal in each gate. Having a complementary input as propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A'B) or implication (A'+B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A+B) function, either choice is equally efficient. Finally, when implementing the NAND (A'+B') or NOR (A'B') function, either choice results to a complementary propagate signal, perforce.

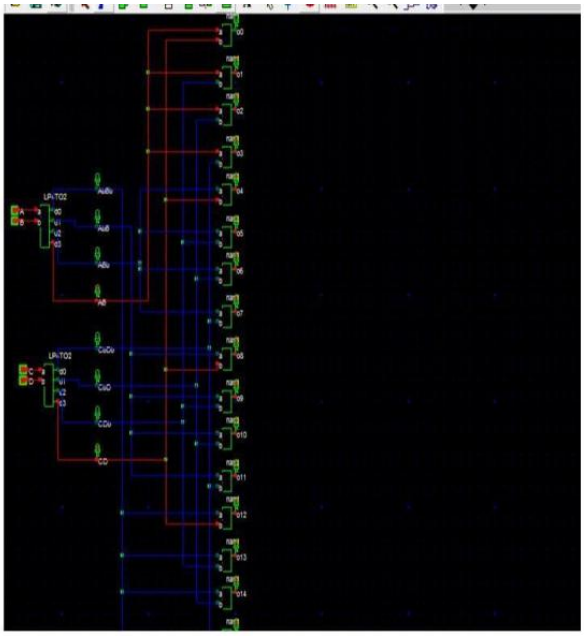

Fig.2. Simulation circuit.

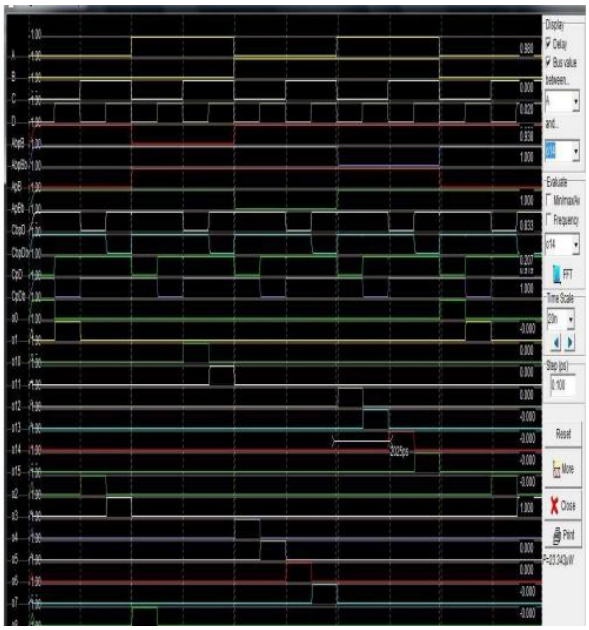

Fig.3. Simulation output.

4. CONCLUSION

This project presented a proficient blended rationale structure for decoder circuits, joining TGL, DVL and static CMOS. By utilizing this procedure, this

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has created four new 2-4 line decoder topologies, specifically 2-4LP, 2-4LPI, 2-4HP and 2-4HPI, which offer lessened transistor check (in this way conceivably littler design region) and enhanced power-defer execution in connection to traditional CMOS decoders. Besides, four new 4-16 line decoder topologies were introduced, in particular 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, acknowledged by utilizing the blended rationale 2-4 decoders as predecoding circuits and joining them with post-decoders actualized in static CMOS rationale. These plans join the enhanced execution attributes of pass transistor rationale with the reestablishing capacity of static CMOS An assortment of similar zest recreations was performed at the 32 nm, checking, as a rule, a clear preferred standpoint for the proposed plans. The 2-4LP and 4-16LPI topologies are generally reasonable for applications where territory and power minimization is of essential concern. The 2-4LPI, 2-4HP and 2-4HPI, and additionally the comparing 4-16 topologies (4- 16LP, 4-16HPI, 4-16HP), ended up being practical and all-around proficient plans, along these lines they can adequately be utilized as building hinders in the structure of bigger decoders, multiplexers and other combinational circuits of differing execution necessities. In addition, the exhibited lessened transistor tally and low power attributes can profit both mass CMOS and SOI configuration also. The acquired circuits are to be executed on format level, making them appropriate for standard cell libraries and RTL structure.

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