

# Optimized Analysis Reversible Vedic Multipliers for HighSpeed Low Power Operations

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**Abstract**— Multiplier design is always a challenging task; however so many novel designs are proposed, the user needs demands much more optimized ones. Vedic mathematics is world renowned for its algorithms that yield quicker results, be it for mental calculations or hardware design. Power dissipation is drastically reduced by the use of Reversible logic. The reversible Urdhva Tiryakbhayam Vedic multiplier is one such multiplier which is effective both in terms of speed and power. In this research we aim to enhance the performance of the previous design. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications.

**Keywords**— *Quantum Computing, Reversible Logic Gate, Urdhva Tiryakbhayam, Optimized Design, TRLIC.*

## I. INTRODUCTION

Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations [2]. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories [1] or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved.

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP place a vital role in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly

looking for new algorithms and hardware to implement them. Vedic mathematics can be aptly employed here to perform multiplication.

The important consideration of any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In [12] a reversible Urdhva Tiryakbhayam Multiplier had been proposed. This paper is an extension of the previous work which tries to optimize the circuit proposed in [12]. The paper is organized as follows: The section II gives the basics of reversible logic along with the literature review. Section III explains the Urdhva Tiryakbhayam algorithm. The section IV describes the modifications of the existing design in order to evolve the optimized design. Section V compares the proposed design with the other non Vedic multipliers as well as the previous Vedic multiplier design and draws a conclusion claiming the versatility of Reversible Urdhva Tiryakbhayam multiplier.

## II. REVERSIBLE LOGIC

### A. Literature review and Significance of reversible logic

Conventional combinational logic circuits are known to dissipate heat for every bit of information that is lost. This is also evident from the second law of thermodynamics which states that any irreversible process leads to loss of energy. Landauer [3] showed that any gate that is irreversible, necessarily dissipates energy, and each irreversible bit generates  $kT \ln 2$  joules of heat where  $k$  is Boltzmann's constant ( $1.38 \times 10^{-23}$  joules/Kelvin) and  $T$  is temperature in Kelvin. Lowering the threshold voltage and management of the power supply are widely applied practices to decrease the energy consumption in any logical operation [23]. However these technologies of lowering the energy consumption will hit a barrier of  $kT$  [24]. In order to alleviate this, techniques such as reducing the temperature of computer and constructing a thermodynamically reversible computer can be used [25].

Frank [25] analyzed that the second option was a better choice. When the temperature of the system reduces to absolute zero, the energy reduces two orders of magnitude but using reversible computing there can be further more reduction that

matches with the theoretical value. The cardinal feature of reversible computing is that electric charge on the storage cell consisting of transistors is not permitted to flow away during transistor switching [26]. This can be reused through reversible computing and hence decrease energy dissipation. Bennett in 1973 [2] showed that an irreversible computer can always be made reversible. Reversible logic circuits naturally take care of heating since in a reversible logic every input vector can be uniquely recovered from its output vectors and therefore no information is lost.

### B. Introduction of Reversible Logic Gates

A Reversible Logic gate is an n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. This not only helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Because of this bijective mapping the output vectors are merely permutations of the input vectors.

Some of the basic reversible logic gates in the literature those are useful in designing the Reversible Urdhva Tiryakbhayam Multiplier are the Feynman [5] Gate—the only 2x2 gate, that is used for fan-out purposes as well as for complementing. It has a quantum cost of one. Peres [6] Gate—a 3x3 gate that is used to produce AND operation as well as EX-OR operation. It has a quantum cost of four. New Fault Tolerant gate (NFT) – is also a 3x3 gate with a quantum cost five. HNG gate which is a 4x4 gate that can be effectively used as a full adder and provides minimum quantum cost implementation. It has a quantum cost of six. BVPPG [11] is a 5x5 gate with a quantum cost of ten. All the mentioned gates are shown in the figure 1.

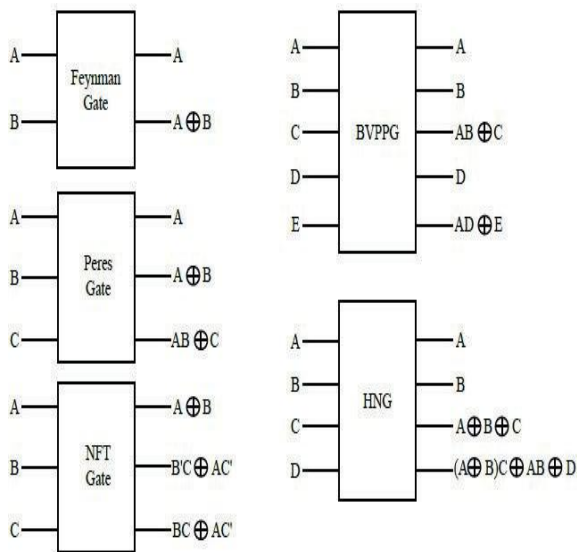


FIGURE 1: REVERSIBLE LOGIC GATES

### C. Optimization parameters for reversible logic circuits

The important parameters [14] which play a major role in the design of an optimized reversible logic circuit are as listed:

- Constants (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Garbage (GO): This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential, without which reversibility cannot be achieved.
- Gate count (NG): The number of reversible gates used to realize the function.
- Flexibility: This refers to the universality of a reversible logic gate in realizing more functions.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit
- Gate levels: This refers to the number of levels in the circuit which are required to realize the given logic functions.
- Total Reversible Logic Implementation Cost (TRLIC) [12]: Let, in a reversible logic circuit there are NG reversible logic gates, CI constant inputs, GO number of garbage outputs, and have a quantum cost QC. Then the TRLIC is given as

$$TRLIC = \sum(NG + CI + GO + QC) \dots 1$$

### III. URDHVA TIRYAKBHAYAM MULTIPLICATION ALGORITHM

Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of clock frequency of the processor. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers.

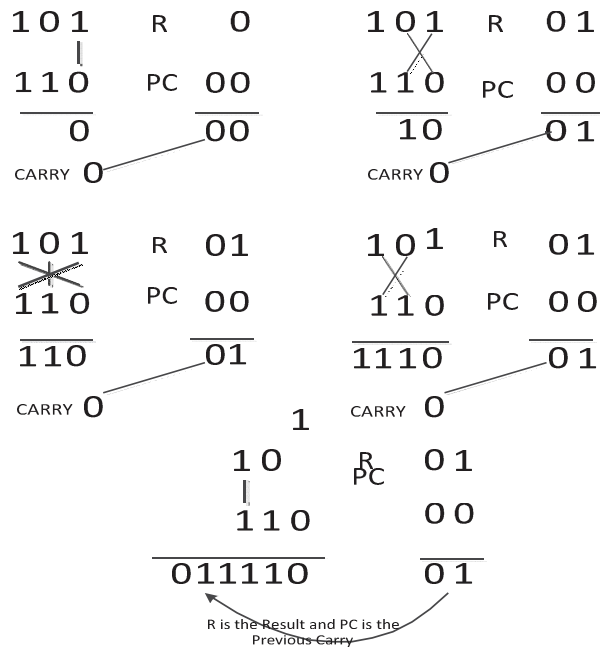


FIGURE 2: URDHVA TIRYAKBHAYAM PROCEDURE FOR MULTIPLICATION

**The Algorithm:** Multiplication of 101 by 110.

1. We will take the right-hand digits and multiply them together. This will give us LSB digit of the answer.
2. Multiply LSB digit of the top number by the second bit of the bottom number and the LSB of the bottom number by the second bit of the top number. Once we have those values, add them together.
3. Multiply the LSB digit of bottom number with the MSB digit of the top one, LSB digit of top number with the MSB digit of bottom and then multiply the second bit of both, and then add them all together.
4. This step is similar to the second step, just move one place to the left. We will multiply the second digit of one number by the MSB of the other number.
5. Finally, simply multiply the LSB of both numbers together to get the final product.

#### IV. OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The conventional logic design implementation of a 2x2 Urdhva Tiryakbhayam multiplier using the irreversible logic gates [8] is shown in the Figure 3. In [12] the four expressions for the output bits are derived from this figure and is used to obtain the reversible implementation as shown in Figure 4. The circuit uses five Peres gates and one Feynman gate. This design has a total quantum cost of 21, number of garbage outputs as 11 and number of constant inputs 4. The gate count is 6. This design does not take into consideration the fan outs. The overall performance of the UT multiplier is

scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs etc.

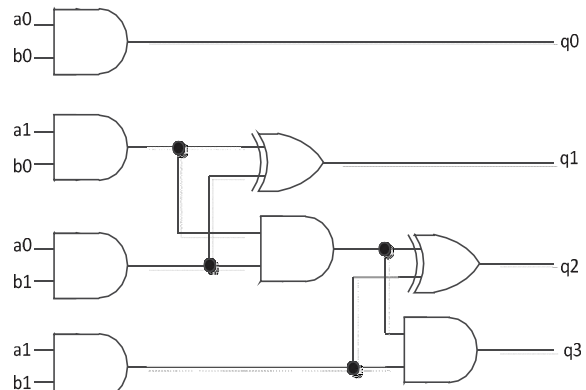


FIGURE 3: CONVENTIONAL 2x2 URDHVA TIRYAKBHAYAM MULTIPLIER [8]

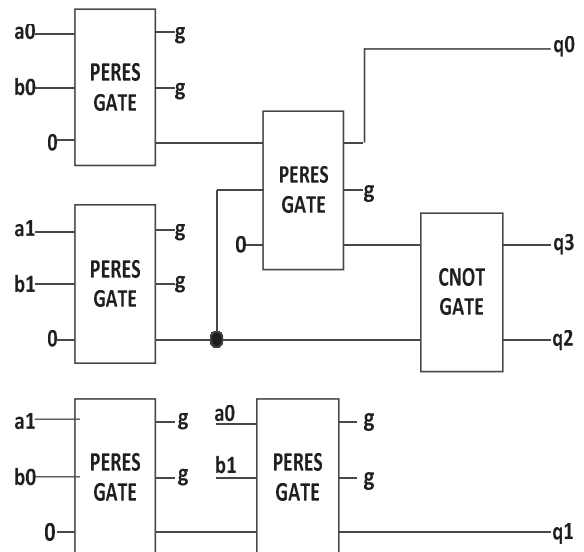


FIGURE 4: REVERSIBLE 2x2 UT MULTIPLIER IN [12]

#### A. Improved 2x2 Urdhva Tiryakbhayam multiplier

The design expressions can be logically modified so as to optimize the design. The new design makes use of one BVPPG, three Peres gates and a single Feynman gate. The design also takes into account the fan outs. One of the major design constraints of reversible logic is the fan out, other being loops not permitted. This means that the reversible logic circuit with multiple numbers of same inputs is not advisable. One way out is to use a separate fan out generator or to build a circuit that inherently takes care of fan outs using the reversible logic gates used in the design. This design has a quantum cost of 23, number of garbage outputs as 5, number of gates 5 and the number of constant inputs is 5.

The second design also considers the fan out using BVPPG, three Peres gates and one NFT gate as shown in the figure 5.

The quantum cost of the circuit is 24; number of garbage outputs as 4, number of gates 5 and the number of constant inputs is 5. I1, I2, I3 (Fig 5 and 6) and I4 (Fig 6) are the intermediate outputs that are used for fan-out purposes.

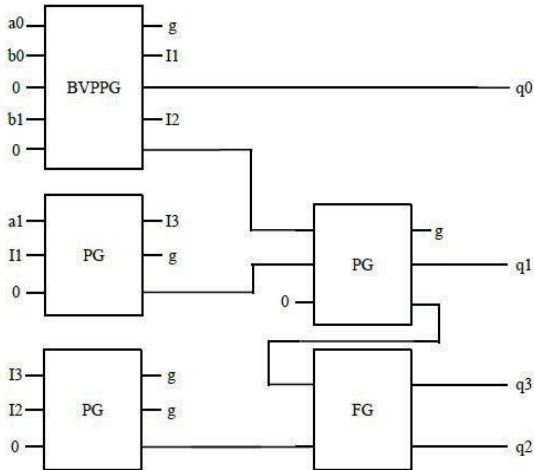


FIGURE 5: PROPOSED MODIFIED DESIGN 1

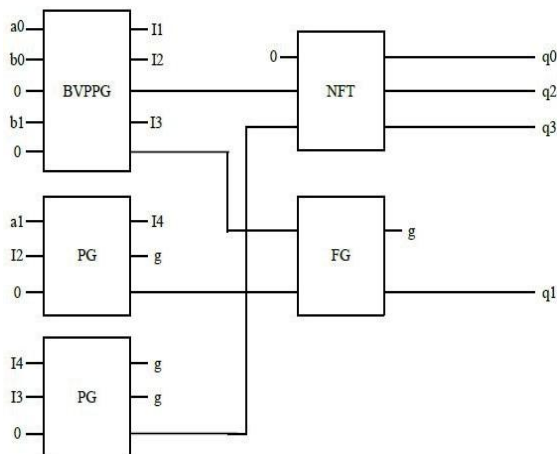


FIGURE 6: PROPOSED MODIFIED DESIGN 2

**B. Design of 4x4 Urdhva Tiryakbhayam multiplier**

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 6. It consists of four 2X2 multipliers each of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up. This is done by a five bit ripple carry adder

which generates a six bit output. These six bits form the upper bits of the final result.

**C. Modification in the design of ripple carry adder**

The design shown in [12] consists of only HNG gates. The number of HNG gates is 4 if the ripple carry adder is used in the second stage or five if the ripple carry adder is used in the last stage of the 4X4 Urdhva Tiryakbhayam Multiplier. The ripple carry adder can be modified as under. Since for any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate can efficiently replace a HNG. This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. The Constant inputs and the gate count remain unchanged.

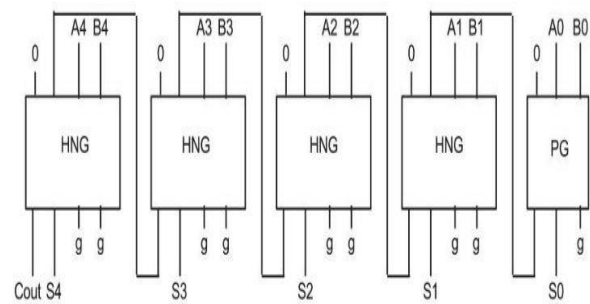


FIGURE 7: PROPOSED MODIFIED 5 BIT RIPPLE CARRY ADDER DESIGN

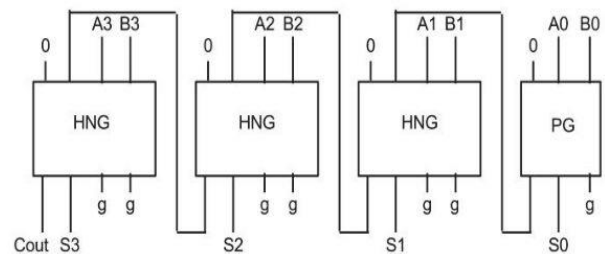


FIGURE 8: PROPOSED MODIFIED 4 BIT RIPPLE CARRY ADDER DESIGN

The 4x4 UT multiplier structure is as shown in figure 9.

**V. RESULTS AND COMPARISONS**

The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figures 10 and 11 respectively. The following are the important design constraints for any reversible logic circuits.

1. Reversible logic circuits should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use a minimum number of reversible gates.

Since TRLIC is the sum of all these design parameters, it is commendable to have a least value of TRLIC. The proposed design of Reversible UT Multiplier is compared with as many as 11 different prominent multiplier designs in the literature in terms of Quantum cost, garbage outputs, number of gates, number of constant inputs and also in terms of TRLIC values. This also includes a comparison with our own previous design and the optimization is clearly evident from the table of Comparison as shown in table 1.

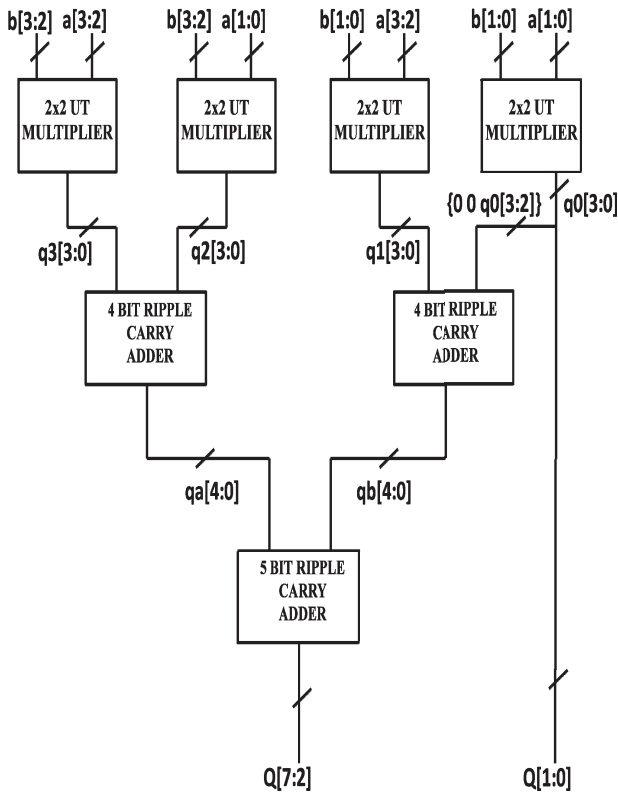


FIGURE 9: BLOCK DIAGRAM OF 4x4 UT MULTIPLIER

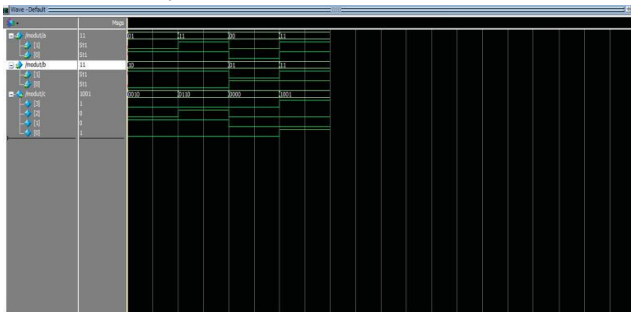


FIGURE 10: SIMULATION RESULTS FOR 2x2 UT MULTIPLIER

The proposed design of 4x4 UT multiplier as already mentioned takes care of the fan-outs also. Though there is a slight increase in the quantum cost of the 2x2 UT multiplier (it is 23 in proposed design 1 and 24 in proposed design 2) as compared to previous [12] design (where it was 21), there is a

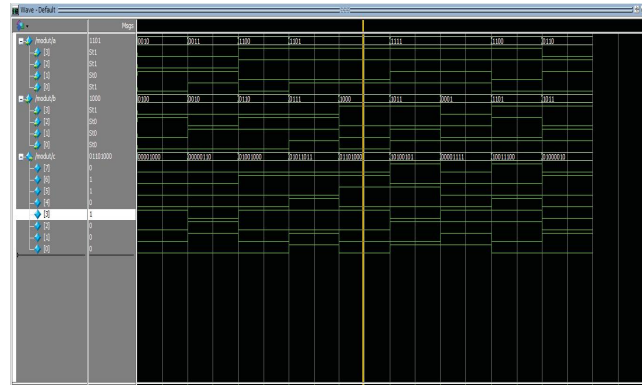


FIGURE 11: SIMULATION RESULTS FOR 4x4 UT MULTIPLIER

substantial decrease in the number of garbage outputs (from 9 to 5 and 4 respectively in designs 1 and 2) and the gate count values (from 6 to 5 in both the designs). Also there is a reduction in the quantum cost of all the ripple carry adders by 2 due to the structural modification involving replacement of first HNG gate by a Peres Gate and reduction in garbage output by one due to the same reason. Therefore, even if the quantum cost has increased slightly, the decrease in the garbage outputs and gate count have totally nullified its effect. The minimum improvement in the TRLIC is at 5.86% which is with respect to [12] and the maximum improvement stand high at 33.6% w.r.t [22]. Also from the table it is clear that both proposed designs have a minimum gate count as well as minimum garbage outputs as compared to all other multipliers studied here. The number of constant inputs is better than 10 of the 11 designs. Thus we can say that the design is very much optimized as compared to others studied here.

**CONCLUSIONS**

The focus of this paper is mainly to design a low power high speed multiplier which is done by constructing the multiplier using reversible logic gates. The procedure is carried out so as to yield an optimized design as compared to those in the literature. The efficiency of a reversible logic circuit is characterized in terms of parameters such as quantum cost, number of constant inputs, garbage outputs and number of gates utilized to realize the logic implementation. Lower the value of these parameters more efficient is the design. In [12] parameter called TRLIC had been proposed which is defined as sum of all cost metrics of the given design. The quantum cost is a parameter that directly reflects the delay of the quantum circuit. Also lower TRLIC implicitly means lower the quantum cost, hence lower is the delay and vice versa. Besides imbibing the design criterion that fan-out must be generated within the circuit, the proposed designs also reduce the TRLIC as compared to the previously proposed design [12]. The further optimization of the circuit in terms of the total logical costs is under progress and is taken as future work.

TABLE I: COMPARISON OF THE PROPOSED MULTIPLIER DESIGNS

Multiplier Designs	No. of Gates	Constant Inputs	Garbage Outputs	Quantum Cost	TRLIC	Percentage Improvement
Proposed 1	33	33	43	164	273	--
Proposed 2	33	33	39	168	273	--
[12]	37	29	62	162	290	5.86%
[13]	40	52	52	152	296	7.77%
[14]	52	52	52	152	308	11.4%
[15]	52	52	52	152	308	11.4%
[16]	52	52	52	152	308	11.4%
[17]	52	52	52	168	324	15.8%
[18]	52	56	56	208	372	26.6%
[19]	44	56	64	236	400	31.8%
[20]	53	58	58	234	403	32.3%
[21]	48	52	64	244	408	33.1%
[22]	64	55	56	236	411	33.6%

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