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RELIABILITY ENHANCEMENT OF LOW POWER TSPC FLIP FLOP

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ABSTRACT:

Flip flop are basic storage elements used extensively in digital system designs, which adopt intensive pipelining techniques and employ several FF-rich modules such as register files, shift registers, and FIFO. The power consumption of the FFs employed in a typical digital system design, along with that of clock distribution networks In this project, an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master–slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual VDD design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the power delay product (PDP).

Keywords: VDD, CMOS, PDP, FF, FIFO.

1. INTRODUCTION

Hardware industry has accomplished an incredible development in the course of the most recent two decades, principally as a result of the quick increments in combination innovations, extensive scale frameworks outline. The utilizations of incorporated circuits have been rising relentlessly which are utilized as a part of elite processing, broadcast

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communications, and buyer gadgets. Normally, the required computational energy of these applications is the main impetus for the quick advancement of this field. An outline of the noticeable patterns in data advances over the coming couple of decades. The present driving edge advances, for example, low piece rate video and cell correspondence. This pattern is relied upon to proceed, with essential applications on VLSI and frameworks outline. A standout amongst the most imperative highlights of data administrations is their expanding requirement for high preparing force and transfer speed. The following vital trademark is that the data administrations turn out to be increasingly customized, for example, communicating, which implies that the gadgets must be more shrewd to answer singular requests and in the meantime they should be convenient to permit greater adaptability/portability. At the point when information handling and media communications gadgets require increasingly complex capacities, they have to coordinate these capacities in a little framework. The quantity of rationale entryways in a solid chip will choose the level of coordination which has been relentlessly expanding for about three decades, which is a direct result of the quick procedure in handling innovation and interconnect innovation. The assessment of rationale multifaceted nature in coordinated circuits in the course of the most recent three decades. The circuit many-sided quality ought to be translated just as delegate cases to demonstrate the request of size. A rationale piece can contain somewhere in the range of 10 to 100 transistors, contingent upon the function.VLSI has been around for quite a while, there is nothing surprising about it, yet as a symptom of advances in the realm of PCs, there has been an emotional multiplication of apparatuses that can be utilized to outline VLSI circuits. Nearby, complying with Moore's law, the ability of an IC has expanded exponentially finished the years, as far as calculation control, usage of accessible zone, yield. The consolidated impact of these two propels is that individuals would now be able to put differing usefulness into the

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IC's, opening up new outskirts. Illustrations are inserted frameworks, where savvy gadgets are put inside regular articles, and universal processing where little registering gadgets multiply to such a degree, to the point that even the shoes you wear may really accomplish something helpful like observing your heartbeats. Verilog was created when fashioners were searching for apparatuses to join diverse levels of reenactment. In the mid1980s, there were switch-level test systems, entryway level test systems, useful test systems (regularly composed specially appointed in programming) and no straightforward intends to consolidate them. Further, the more-broad, conventional programming dialects themselves were/are basically consecutive and in this way "semantically tested" when displaying the simultaneousness of computerized hardware. In 1989, Gateway Design Automation (and rights to Verilog) was obtained by Cadence who place Verilog in the general population space in the next year. This move did much to advance the utilization of Verilog since different organizations could create choices devices to those of Cadence which, thus, enabled clients to embrace Verilog without reliance on a solitary (essentially workstation-device) provider. In 1992, work started to make an IEEE standard (IEEE-1364) and in December 1995 the last draft was endorsed. Along these lines Verilog has turned into a n worldwide standard - which will additionally build its business advancement and utilize. At show, there is benchmarks movement to expand Verilog past simply computerized circuits.

2. LITERATURE SURVEY

In literature many designs have been proposed for the flip-flops. Several techniques as well as various flip-flops have been proposed recently to reduce redundancy in clock system. There are many flipflops given in the literature [8]-[10]. Many digital and computational circuits selectively use master – slave and pulsed triggered flip-flops [6]. The paper presents small area dynamic TSPCL (True Single Phase Clocked Logic) D flip-flops that were presented in [5] and [7]. These edge triggered flipflops are small in area since they exhibit low transistor count. With a simple modification, the internal switching at some nodes of these flip-flops is

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minimized in order to reduce power consumption [7]. TSPCL dynamic logic style uses just a single clock signal for synchronization and it also reduces complexity. In the design of TSPC flip-flop edge triggered (positive or negative) D flip-flop is used. The circuit consists of alternating stages called n-blocks and pblocks and each block is being driven by the same clock signal. The schematic of original TSPC flipflop is shown in Fig.1. In this design a single global clock signal needs to be generated and distributed in order to simplify the design. Fig.1 Shows the Conventional d flip flop in dsch schematic, Fig .2 shows the schematic of TSPC D flip-flop with 10 transistors, this edge triggered flip-flop uses just a single clock signal for synchronization. It is operated as when the clock signal clk is LOW, the input is isolated from the output. When clock makes a LOW-to-HIGH the output will latch the complement of the input.

EXISTING SYSTEM:

This existing system enumerates a low power, high speed design of flip-flop having less number of transistors. In flipflop design only one transistor is being clocked by short pulse train which is known as True Single Phase Clocking (TSPC) flip-flop. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds. In this paper, an extensive comparison of existing designs of positive edge triggered True Single Phase Clocking Flip-flop is carried out. As True Single Phase Clocking (TSPC) flip-flop design has small area and low power consumption. And it can be used in various applications like digital VLSI clocking system, microprocessors, buffers etc. The analysis for various flip-flops for power dissipation and propagation delay has been carried out at different foundries.

3. AN OVERVIEW OF PROPOSED SYSTEM

As indicated in the MOS schematic shown in Fig.2. the converged discharging path controlled by x2/x3 and CK in the slave latch is first split into two separate discharging paths, each comprising two nMOS transistors in series and implementing the logic x2·CK·0 and x3·CK·0. If x2 = 1 (or x3 = 1),it is logically equivalent to $\bar{}$ x2 ·CK (or $\bar{}$x3 ·CK). Because x2 and x3 are complementary, $\bar{}$ x2 ·CK = x3 ·CK (or $\bar{}$ x3 ·CK = x2 ·CK). As indicated in the small figure in Fig. 3.14 this term can be

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implemented using one pass transistor with CK as the control signal and x3 (or x2) as the sink of the discharging current. The converged discharging path in the TCFF design can be split into two separate paths, each comprising one pass transistor. Because these two pass transistors operate in a complementary manner, they are considered as CPL, and the transistor count can thus be reduced by one. The benefit of this logic structure reduction is twofold. First, it simplifies the circuit for power saving. Although the pull down delay might be slightly prolonged, it does not correspond to the worst case timing (in contrast to the pull-up delay). Second, when node x2 (or x3) is equal to 1, the pass transistor works in conjunction with the pull-up path formed by pMOS transistors p3/p4 (or p5/p6) to boost the output node of AOI to 1. This path is considered auxiliary because a "weak 1" can be delivered by an nMOS pass transistor. This additional current boost, however, improves the worst case delay when the slave latch is in the transparent mode (CK = 1). A shorter clock-to-Q (CQ) delay can be obtained. The dotted and solid arrowed lines in Fig. 3.14 indicate the working of these two charging paths to drive node x5 (or x4). The second logic structure reduction scheme is applied to the second AOI gate of the master latch. The discharging path of node x2 controlled by CK and x3 discharges only when both signals equal 1. As illustrated in Fig. 3.18 pass transistor n7in addition to pull-down transistor n8 controlled by x4 forms an alternative discharging path for node x2. This can thus remove the original (and redundant) path to simplify the circuit. This measure not only improves the power performance but also reduces the capacitive load of node x2. A shorter propagation delay can be achieved for the master latch when operating in the transparent mode, resulting in a shorter setup time of the FF design. The circuit schematic after the application of the two logic structure reduction schemes is presented in Fig. 3.19. The total number of transistors is only 19. Only one single

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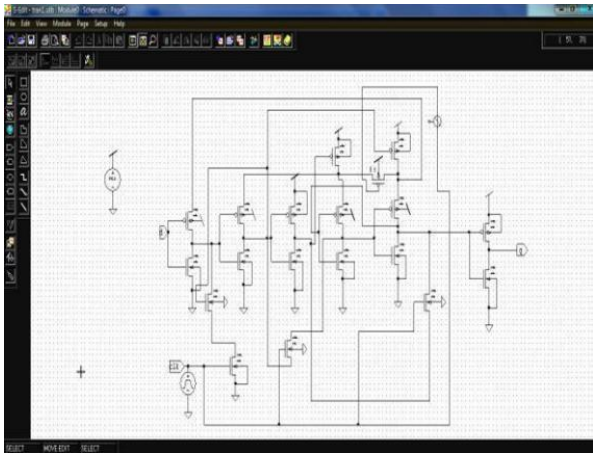

Fig.1. Circuit connection of Master- slave D-flip-flop using TCFF technique.

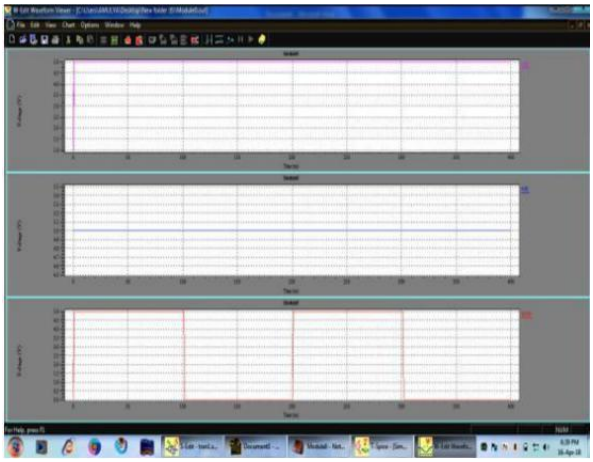

Fig.2. Simulation wave forms low power 19-transistor true single phase clocking using reduction schemes.

4. CONCLUSION

This present a novel FF design achieved by employing a modified SR latch structure incorporating a hybrid logic consisting of static-CMOS logic and CPL. The key idea is providing an additional discharge path between the master and slave latches, which not only shortens the transition time to enhance the power and speed performance, but also reduces circuit complexity for better timing parameters. Extensive simulations were conducted and various performance indices such as power consumption, PDP, setup time delay, and CQ delays were evaluated. The proposed design was determined to excel in almost every performance index, except for hold time performance. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design. This hope that presented results will encourage further research activities in TCFF technique. The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility. More work was recently done in automation of logic design methodology based on TCFF technology.

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