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The Method of Low Power, High Performance and Area Efficient Address Decoder Design for SRAM

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Abstract— In this paper a new method of design of CMOS decoder circuit was proposed. To minimize power consumption and increase the performance of the design the following design solutions have been Designed The New Technique used Is Gate Diffusion Input (GDI) which need Two transistor for design of Basic gates like AND,OR gates which are used in Decoders .In this project the GDI 2-4 and 4-16 Decoder is designed and Compared with the Existing Design which is mixed-logic design method, combining transmission gate logic, dual-value logic pass-gate transistor . Three schematics are presented in the project according which 2-4 decoders were designed. In the first solution a 12-FET based circuit with GDI and 14-FET based LP Decoder and 15-FET Hp Decoders was designed which can be used to minimize the area and power consumption of digital VLSI ICs. The 12-FET based circuit was also proposed to increase the performance of digital ICs with reference to 14-FET and 15-FET based solution. Using the above-mentioned cells, the following more complex digital decoders have been designed: like 4-16 decoders. The above GDI proposed solutions have shown better performances, lower power consumptions and less required area of silicon compared to the ones currently used in digital designs. The proposed solutions have been analyzed in TANNER EDA Software.

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary NMOS pulldown and PMOS pull up networks and present good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates.

This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including. In digital electronics, a binary decoder is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs. They are used in a wide variety of applications, including data demultiplexing, seven segment displays, and memory address decoding.

There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple input and multiple output signals, which converts every unique combination of input states to a specific combination of output states. In addition to integer data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states.

Depending on its function, a binary decoder will convert binary information from n input signals to as many as 2^n unique output signals. Some decoders have less than 2^n output lines; in such cases, at least one output pattern may be repeated for different input values.

A binary decoder is usually implemented as either a stand-alone integrated circuit (IC) or as part of a more complex IC. In the latter case the decoder may be synthesized by means of a hardware description language such as VHDL or Verilog. Widely used decoders are often available in the form of standardized ICs.

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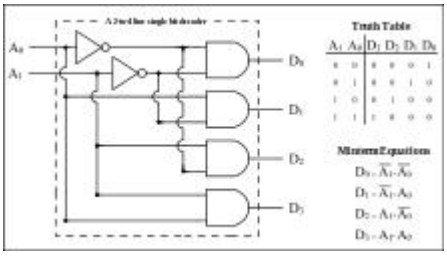

Figure-1: A 2-to-4 line decoder

A 1-of-n binary decoder has n output bits. This type of decoder asserts exactly one of its n output bits, or none of them, for every integer input value. The "address" (bit number) of the activated output is specified by the integer input value. For example, output bit number 0 is selected when the integer value 0 is applied to the inputs.

II. RELATED WORK

Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products. An implemented 32-b adder using complementary CMOS has a power-delay product of less than half that of the CPL version. Robustness with respect to voltage scaling and transistor sizing, as well as generality and ease-of-use, are additional advantages of CMOS logic gates, especially when cell-based design and logic synthesis are targeted. This paper shows that complementary CMOS is the logic style of choice for the implementation of arbitrary combinational circuits if low voltage, low power, and small power-delay products are of concern.

A 3.8-ns, 257-mW, 16*16-b CMOS multiplier with a supply voltage of 4 V is described. A complementary pass-transistor logic (CPL) is proposed and applied to almost the entire critical path. The CPL consists of complementary inputs/outputs, an nMOS pass-transistor logic network, and CMOS output inverters. The CPL is twice as fast as conventional CMOS due to lower input capacitance and high logic functionality. Its multiplication time is the fastest ever reported, even for bipolar and GaAs ICs, and it can be enhanced further to 2.6 ns with 60 mW at 77 K.<>

Guided by the switch-signal theory, this paper introduces design theory suitable for current-mode CMOS circuits at switch level. On this basis, the operations of current transmission switch used to describe the action of threshold-controllable switch in Schmitt trigger are established, and a novel current-mode CMOS ternary Schmitt trigger with ternary output current or/and voltage signal is presented. The two hysteresis current values of ternary Schmitt trigger are controlled by only sizing the transistor aspect ratio. The main properties of the circuit are its simple structure, fully adjustable hysteresis and suitable for low-voltage applications. A design example and the HSPICE simulation results with a power supply of 1.5V are given

This paper presents new pass-transistor logic termed DVL which contains fewer transistors than its counterpart DPL yet maintaining comparable performance. A method for synthesis of such networks is also developed and demonstrated in this paper. The new logic is characterized by good speed and low power. The simulations and tests were performed using 1-/spl mu/m CMOS.

III. EXISTING SYSTEM

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the m = 2n minterms of n input variables. At a small scale, circuits based on pass transistor logic can realize logic functions with fewer transistors and improved performance compared to static CMOS. However, cascading several non-restoring circuits causes a rapid degradation in performance. A mixed-topology approach, ie alternating restoring and non-restoring levels of logic, can potentially deliver optimum results, combining the positive characterists of both.

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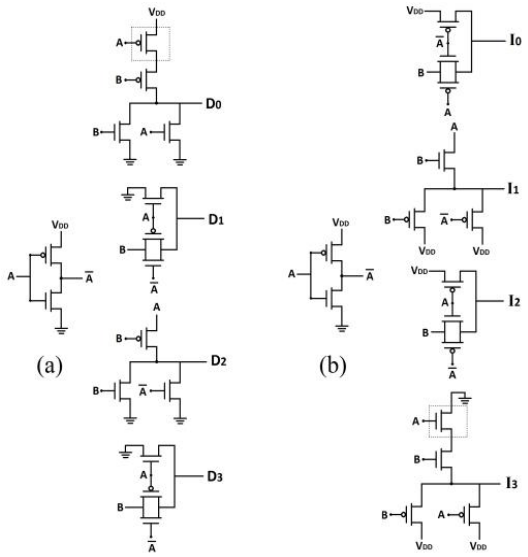

Figure-2: New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI

IV. PROPOSED SYSTEM

The proposed system Speed digital system, digital signal processing or control system. The primary issues in the design of adder cell are area, delay and power dissipation. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. This paper mainly presents the design of 5 different full adder topologies using Modified Gate Diffusion Input Technique. This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. This paper focuses two main design approaches. The former presents the implementation of modified primitive logic cells and its performance issues were compared with GDI and CMOS logic. The latter presents the implementation of 5 different modified GDI full adders and its performance issues. The simulation results reveal better delay and power performance for the proposed modified GDI full adders when compared with the existing GDI technique, CMOS and pass transistor logic at 45 nanometer CMOS technologies. Delay and power has been evaluated by Tanner simulator using TSMC BSIM 45 nanometer technologies.

To reduce the power consumption different logic design techniques like CMOS complementary logic, Pseudo nMOS, Dynamic CMOS, Clocked CMOS logic (C2 MOS), CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed. Although Static CMOS Logic has been the most popular design approach for the past three decades, many attempts have been made to propose a better alternative to achieve lower power dissipation, smaller area and better performance reported in Circuit designed with transmission gate (TG) solves the problem of low logic level swing by using PMOS as well as NMOS but this implementation needs true and complemented control signal and requires more area than pass transistor logic. Pseudo-NMOS is simple and fast but reduces noise margins and increases power consumption. Pass-transistor logic is good for certain classes of circuits (MUX/adders). On the other hand, PTL implementations of logic gates such as NANDs and NORs were found to be slower and consume more power than CMOS implementations mainly because of the reduced output swings due to the threshold drop across a single-channel pass transistor.

a) GDI primitive cells

The basic primitive of GDI cell consists of nMOS and pMOS containing four terminals G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of MOS transistor), and D (common diffusion node of both transistors). In this work a modified primitive GDI logic gates have been implemented in 0.250µm technology and it is compared with existing GDI and CMOS logic. Figure shows the construction of modified GDI basic gates of AND, OR, NOR, NAND, XOR, XNOR and MUX. As an example the operation of AND gate is elucidated. For AND gate the drain of pMOS is -off. -off and nMOS in linear pMOS in linear and nMOS in cut-off linear and nMOS in linear thereby producing the output as 1. The logical level for different input combination will be:

For A=0 and B=0: pMOS in Linear: Vin Vtp < Vout < VDD. nMOS in Cut-off: Vin<Vtn

For A=1 and B=0: pMOS in Cut-off: Vin > VDD + Vtp. nMOS in Linear: 0 < Vout < Vin – Vtn

For A=0 and B=1: pMOS in Linear: Vin Vtp < Vout < VDD. nMOS in Cut-off: Vin<Vtn

For A=1 and B=1: pMOS in linear: Vin Vtp < Vout < VDD. nMOS in linear: 0 < Vout < Vin - Vtn

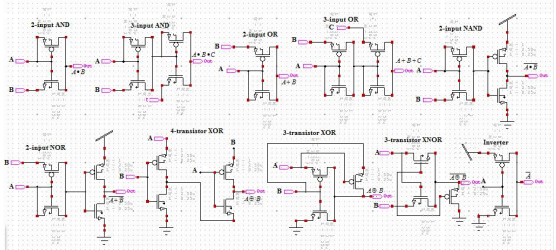

Figure-3: GDI primitive logic gates

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The performance analysis of GDI and CMOS logic is presented. The performance evaluation is made with respect to switching delay, transistor count and average power consumed by MGDI, GDI and CMOS logic. From this analysis it is observed that the modified GDI performance is better when comparing to GDI and CMOS logic.

b) Design of GDI Full adders

A full adder is a combinational circuit that performs the arithmetic sum of three bits: A, B and a carry in, C, from a previous addition produces the corresponding SUM, S, and a carry out, CARRY. The various equations for SUM and CARRY are given below. Five different GDI full adders have been designed with transistor count of 16T, 14T, 12T, 10T and 8T. For 16T GDI full adder implemented from the eq 1 & 2, the sum expression is designed using 3-input XOR gate, whereas carry expression is designed using 2-input AND and 3-input OR gate. Similarly for 14T GDI full adder from the eq 3 & 4, the sum is implemented with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is implemented with 2-input AND and 2-input OR gate. For 12T GDI full adder from the eq 5 & 6, sum is realized using 3-input XOR gate and carry is realized using 2-input OR and 2-input AND. The 10T MGDI full adder from the eq 7 & 8, sum is designed with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is designed with 2-to-1 MUX. Finally 8T GDI full adder from the eq 9 & 10, has been realized using 3-input XOR for sum expression and for carry expression 2-to-1 MUX have been used. The proposed 5 different GDI full adders are simulated using Tanner EDA with BSIM3v3 250nm technology with supply voltage ranging from 1V to 5V in steps of 0.5V. All the full adders are simulated with multiple design corners (TT, FF, FS, and SS) to verify that operation across variations in device characteristics and environment. The design of 5 different full adders using GDI is shown in above figure.

$$SUM = A \oplus B \oplus C \quad (1)$$
$$CARRY = AB + BC + AC \quad (2)$$
$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B}) \quad (3)$$
$$CARRY = \overline{C}(AB) + C(A + B) \quad (4)$$
$$SUM = A \oplus B \oplus C \quad (5)$$
$$CARRY = (A \oplus B)C + AB \quad (6)$$
$$SUM = \overline{C}(A \oplus B) + C(\overline{A \oplus B}) \quad (7)$$
$$CARRY = (\overline{A \oplus B})B + (A \oplus B)C \quad (8)$$
$$SUM = A \oplus B \oplus C \quad (9)$$
$$CARRY = (\overline{A \oplus B})B + (A \oplus B)C \quad (10)$$

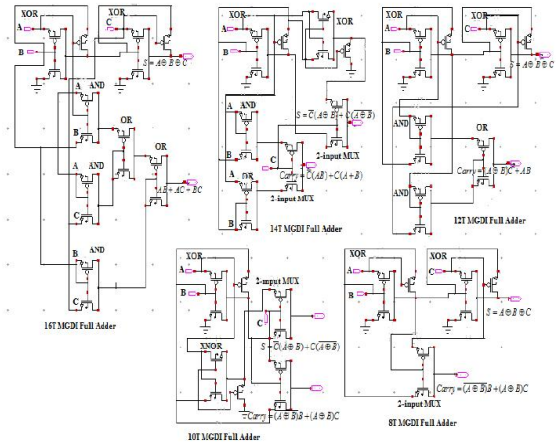

Figure-4: GDI Full adders

V. RESULTS

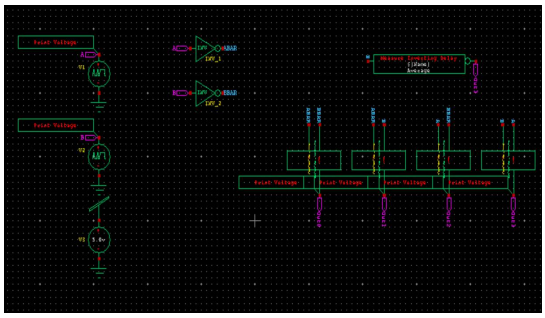

Figure-5: Proposed Circuit 12T 2-4 Decoder

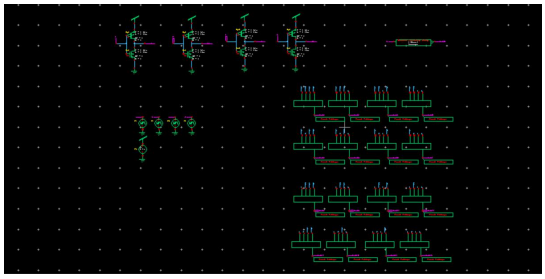

Figure-6: Proposed Circuit 4-16 Decoder

VI. CONCLUSION

The proposed decoders are asymmetric and need to be properly connected to avoid hazards. For the correct connection of the inputs, a method has been developed in TCL language, which allows to make the most of the advantages of proposed asymmetric circuits.

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