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VLSI Implementation of Turbo Coder for LTE Using Verilog HDL

Ms. L. Lavanya (Assistant professor)

SAI CHARAN BHUPATHI (188R1A0451), T BHADUR BHANDARI (188R1A0453), T KRANTHI KALYAN (188R1A0454), TUMMA SUPRIYA (188R1A0457)

Department of ECE, C M R Engineering College,Hyderabad, Telangana, INDIA

ABSTRACT

Turbo codes are error correction codes that are widely used in communication systems. Turbo codes exhibits high error correction capability as compared with other error correction codes. It proposes a Very Large-Scale Integration (VLSI) architecture for the implementation of Turbo decoder. Soft-in-soft out decoders, interleavers and de-interleavers is used in the decoder side which employs Maximum-a-Posteriori (MAP) algorithm. The number of iterations required to decode the information bits being transmitted is reduced by the use of MAP algorithm. For the encoder part, this uses a system which contains two Recursive convolutional encoders along with pseudorandom interleaver in encoder side. Turbo codes is one of existing powerful error correcting codes. Turbo codes has inspired the coding community with the possibility of using an iterative decoding technique that relies solely on simple constituent code to achieve close channel capacity. The Turbo encoding and decoding is done using Octave, Xilinx Webpack, Cadence tools. The system is implemented and synthesized in Application Specific Integrated Circuit (ASIC).

I. INTRODUCTION

In a communication system, when data is transferred from the source system to a destination system, errors can be present in the received signal at the source end. So error correction is required to retrieve the original message. Turbo codes, which were first introduced in 1993, represent a quantum leap in channel coding techniques and a turning point for modern digital telecommunication. Turbo codes is one of existing powerful error correcting codes. Turbo codes has inspired the coding community with the possibility of using an iterative decoding technique that relies solely on simple constituent code to achieve close channel capacity. Turbo coder architecture comprises of turbo encoder and turbo decoder. Encoder consists of two Recursive Convolutional Encoders (RSC) and interleaver. In this pseudo-random interleaver is used due to which the interleaved version of the code tends to be long and scrambled, that gives good performance of random codes. In turbo code implementation, RSC encoders are employed rather than conventional convolutional encoders since it generates low weight parity codes. MAP algorithm is used for the decoding of turbo encoded data in which errors are intentionally added and verified an error free decoded data after decoding. Turbo codes, capable of achieving close-to-Shannon capacity

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and amenable to hardware-efficient implementation, have been adopted by many wireless communication standards, including HSDPA and LTE. The turbo encoder specified in the LTE standard is illustrated in Figure 1 and consists of a feed-through, two 4-state recursive convolutional encoders (CEs), and an interleaver. LTE employs a rate 1/3 parallel concatenated turbo code. The corresponding encoder is comprised of two rate 1/2 recursive systematic convolutional encoders, as shown in Figure 1. The first component encoder receives un-coded (systematic) data bits in natural order and outputs a set of parity bits x. The second CE receives an interleaved sequence of the information bits, where stands for the interleaved address associated with address, and generates a second sequence of parity bits. The systematic bits and the two sets of parity bits are then modulated onto an analog waveform (according to the employed communication 14 standard) and sent over the radio channel. On the other side of the wireless link, a demodulator is responsible for the reconstruction of the transmitted bits from the received signal. However, since this signal is usually distorted by noise and interference, the demodulator can only obtain estimates of the systematic and two sets of parity bits. These estimates are provided to the subsequent turbo decoder in the form of loglikelihood ratios (LLRs), and which express the ratio between the probabilities of the transmitted bits being 0 and being 1, given the received analog signal. Turbo codes are designed in such a way that an interleaver is used between the two encoders which are connected parallelly, as shown in figure 1. The presence of an interleaver will be used to generate very large codeword length with good performance, at low SNRs. And even which are possible to achieve the Shannon limit which is nearly equals to 0.7dB. The turbo encoders are formed with the help of two RSC encoders in which they are separated by an interleaver, of length N. The RSC encoders used are systematic as the input bit will also occur at the output which will generates N-information bits as the inputs are followed by the parity bits. The interleaver place an important role in the turbo codes. Turbo codes are mainly designed for the burst errors, in which the interleaver helps in removing the errors. Turbo encoder is designed with the help of an interleaver. It is also helpful for maintaining the BER performance by regularly changing the size of an interleaver. In turbo code, random interleaver is used for rearranging the data bits without any repetition. At both the encoding and decoding side the Interleaver is used. The interleaver improves the code error performance at moderate to high signal-to-noise ratio. It generates a long block of data at the encoder side, at the output it connects two decoders and helps in correcting the errors. When the encoded data passes from the first decoder, only some of the errors got corrected. Then the received message from first decoder has been sent through the interleaver, interleaved output of the first decoded data is passes to the second decoded data, then the remaining errors get corrected, then the same procedure has been repeated number of times. The interleaver is able to give the random values and that will help to give the parity bits from each of the RSC encoders which are independent. These parity bits depend on the length or depth of an interleaver

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II. EXISTING METHOD

Convolutional coding is a coding scheme used in communication systems including deep space communications and wireless communications. It provides an alternative approach to block codes for transmission over a noisy channel. The block codes can be applied only for the block of data. The convolutional coding has an advantage over the block codes in that it can be applied to a continuous data stream as well as to blocks of data. IS-95, a wireless digital cellular standard for CDMA (Code Division Multiple Access), employs convolutional coding. A third-generation wireless cellular standard, under preparation, plans to adopt turbo coding, which stems from the convolutional coding. The Viterbi decoding algorithm was proposed and analyzed by Viterbi in 1967. It is widely used as a decoding technique for convolutional codes as well as the bit detection method in storage devices. Viterbi decoders currently find their use in more than one billion cell phones. The algorithm works by forming trellis structure, which is eventually traced back for decoding the received information. Convolutional encoding with Viterbi decoding is a powerful method for forward error correction. The Viterbi algorithm essentially performs maximum likelihood decoding. However, it reduces the computational complexity by using trellis structure. The convolutional encoder and Viterbi decoder, which is used in the digital communication system. A Viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. The maximum likelihood detection of a digital stream is possible by Viterbi algorithm. In this, we present a Convolutional encoder and Viterbi decoder with a constraint length of 7 and code rate of 1/2.Here, X is the input data steam, which is given into the convolutional encoder and it produces the encoded data stream (Y). The encoded data stream (Y) is given to the channel in the presence of noise. Hence, it produces the noise added encoded data stream (R). Finally, data stream (R) is given to the Viterbi decoder that produces the estimated data stream (Z) applied at the input.

2.1 CONVOLUTIONAL ENCODER

Convolutional codes are very suitable to protecting the digital data transmission from random errors due to any noise source. It achieves error free transmission by adding sufficient redundancy to the source symbols. Convolutional codes are usually described using two parameters: the code rate and the constraint length. The code rate is expressed as a ratio of number of input symbols (k) into the channel encoder to the number of output symbols (n) by the channel encoder in a given cycle. Then, the code rate is expressed as, r = k/n bits/symbol The constraint length (K) denotes the length of the convolutional encoder. Convolutional encoder increases the length of the message sequence by adding redundant bits in order to increase the likelihood of detecting the transmitted sequence even if errors have occurred during transmission. Figure 2 shows the convolutional encoder of constraint length (K) = 7 and code rate (r) = 1/2. A convolutional encoder generates redundant bits by using modulo-2 convolutions. Hence, it is called as Convolutional

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encoder. If n modulo-2 adders are used, then it produces n outputs for each bit.

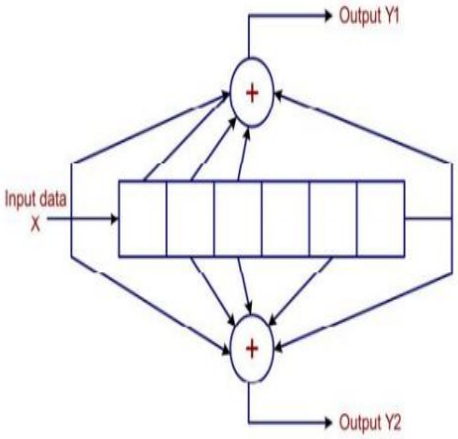

Fig 2.1.1: Constraint length (K)=7, code rate (r)=1/2 convolutional encoder

2.2 VITERBI DECODER

Viterbi algorithm is used in the Viterbi decoder for decoding a bit stream that has been encoded using FEC based on a Convolutional code. It consists of the following functional units, namely, Branch Metric Unit, Path Metric Unit, Survivor Memory unit.

2.2.1: Branch Metric Unit

The comparison between received code symbol and expected code symbol is done by branch metric unit. It also counts the number of differing bits. It is the smallest unit in the Viterbi decoder. The measured value of the BMU can be the Hamming distance in case of the hard input decoding or the Euclidean distance in case of the soft input decoding.

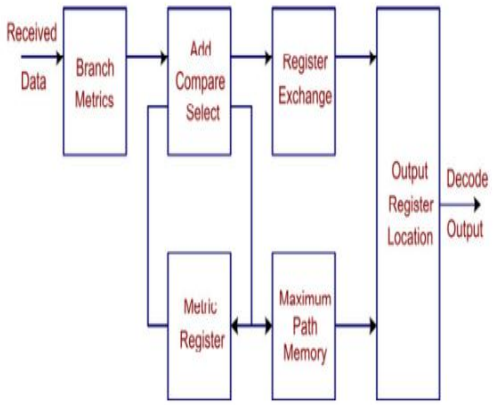

Fig 2.2.1 Block diagram of Viterbi decoder

III. PROPOSED METHOD

3.1 ARCHITECTURE OF TURBO CODER

Turbo encoder and decoder together comprises the Turbo coder architecture (shown in figure. Two identical Recursive convolutional encoders (RSC) and a pseudorandom interleaver constitutes the turbo encoder LTE employs a 1/3 rate parallel concatenated turbo code. Each RSC works on two different data. Original data is provided to the first encoder, while the second encoder receives the interleaved version of the input data. A specified algorithm is used to scramble the data bits and the method is called Interleaving. An appreciable impact on the performance of a decoder is seen with the interleaving algorithm when used. This will be transmitted through the channel to the Turbo decoder. A standard turbo decoder block diagram that contains two modules of SISO decoders together with two pseudorandom interleavers and a

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pseudorandom de-interleaver.

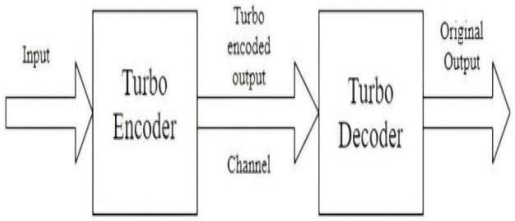

Fig 3.1.1: Turbo Coder Block diagram

The RSC1 and RSC2 encoder outputs along with systematic input comprises the output of turbo encoder, that is, a 24-bit output is generated. The usually used method of turbo code decoding is carried out using the BCJR algorithm. The fundamental and basic idea behind the turbo decoding algorithm is the iteration between the two SISO part decoders. For turbo codes, an interleaver is used between the two component encoders. The interleaver is used to provide randomness to the input sequences. For both serial and parallel concatenation schemes, an interleaver is often used between the encoders to improve burst error correction capacity or to increase the randomness of the code. It comprises a pair of decoders, those which work simultaneously in order to refine and upgrade the estimate of the original information bits. The first and second SISO decoder, respectively, decodes the convolutional code generated by the first or second turbo-iteration corresponds to one pass of the first component decoder which is followed by a pass of the second component decoder.

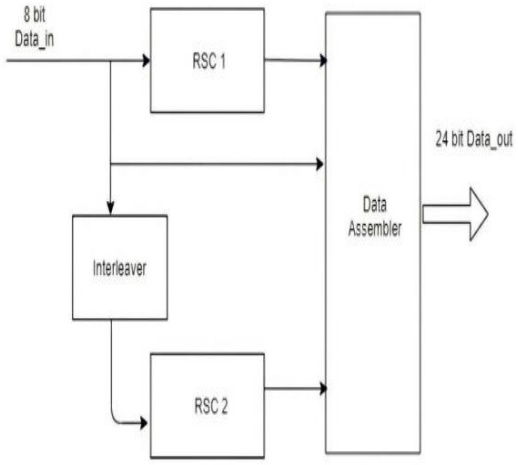

Fig 3.1.2: Turbo Encoder Block Diagram

3.2 SISO DECODER

The signal which is received at the input of a soft-in-soft out (SISO) decoder is the real (soft)value of that signal.

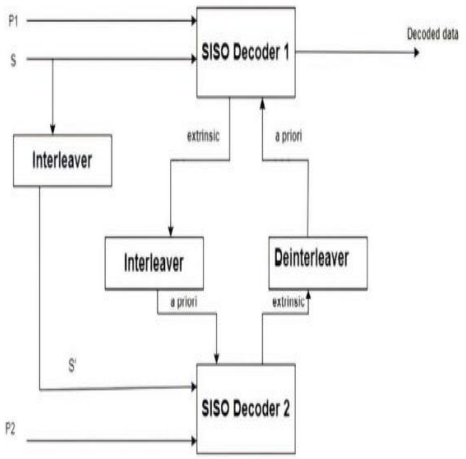

Fig3.1.3: Turbo Decoder Block diagram

An estimate of each input bit the decoder then generates an approximation for each data bit expressing the probability that the transmitted data bit is equal to one. The maximum a-posteriori (MAP) algorithm is used in the turbo-decoder under consideration for the SISO component decoder.

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4.3 INTERLEAVER

Choosing the interleaver is a significant part of the turbo code design. Interleavers scramble data in a pseudorandom order to lessen the resemblance between adjacent bits at the input of the convolutional encoder. The interleaver is used on both the encoder part and the decoder part. It produces a long block of data on the encoder side, while it compares two SISO decoders'

output in the decoder portion and helps to fix the error. Pseudo-random de-interleaver functions in a complimentary manner of pseudo-random interleaver.

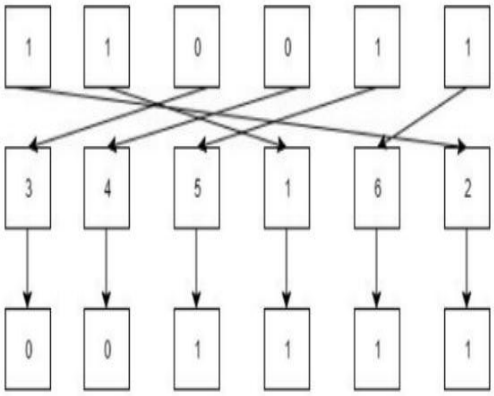

Fig 3.1.4: Pseudo-random interleaver working principle

3.4 MAP ALGORITHM

The MAP algorithm minimizes the likelihood of bit error by using the entire sequence that was obtained to figure out the most likely bit at each trellis point. Consider a frame of N coded symbols consisting of m bits and the channel output received by the decoder as y. For every dsym i, a MAP decoder provides a 2m a posteriori probability.

VI. RESULT

TURBO ENCODER

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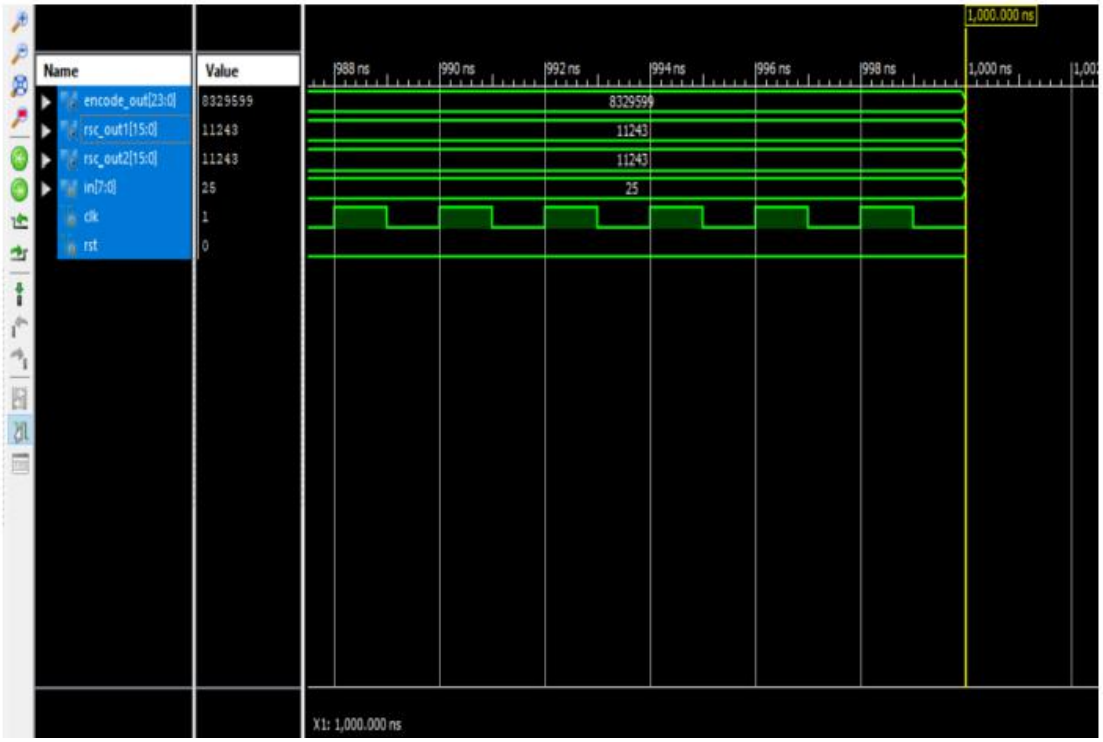

Fig 4..1: Turbo encoder Simulation

TURBO DECODER

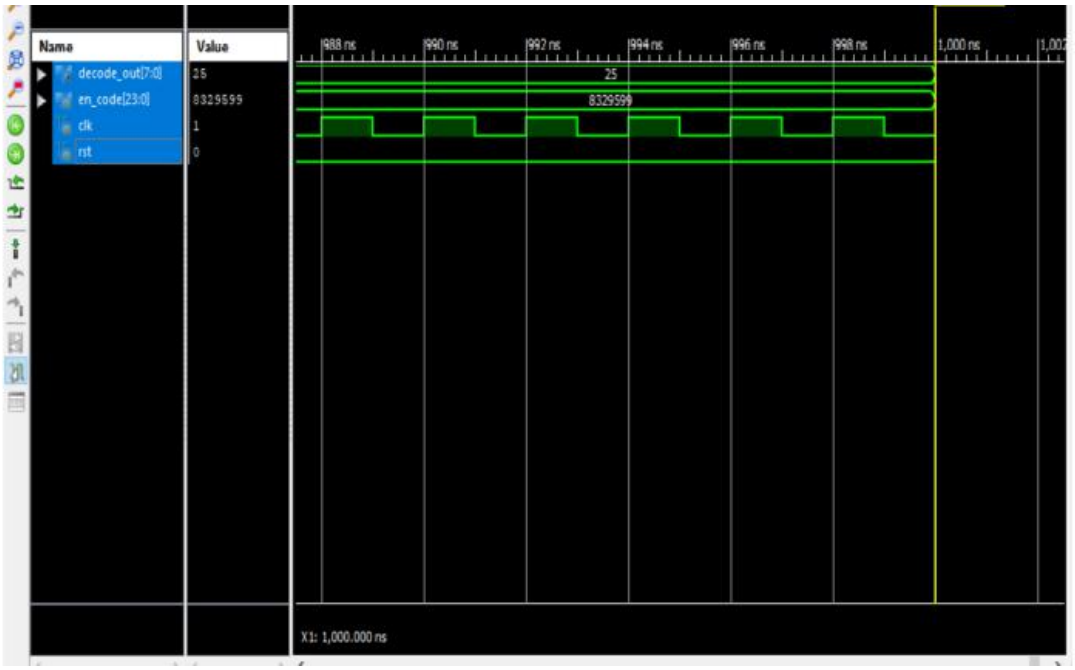

Fig 4.2: Turbo decoder Simulation

V. CONCLUSION:

Turbo encoding and decoding is done using Verilog HDL. The decoder is

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developed based on MAP algorithm. Layout of Turbo decoder algorithm identifies the most probable bit of information that was sent. Original MAP algorithm is used because the number of iterations for process decoding is reduced. Many approximations on the MAP algorithm are usable, such as the Max-Log MAP algorithm, where computations are mostly in the logarithmic realm, thus facilitating the implementation of values and operations. Here, the decoder successfully corrects the error and retrieves the original message. Synthesis is done in Xilinx -webpack, results are tabulated and synthesis report is being generated. Encounter tool is used to convert the netlist to physical design. Floor planning, placement and routing are performed. GDS II file has been generated successfully.

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