

ANALYSIS OF AN INTEGRATED BUCK - ZETA CONVERTER

¹M. JYOTHI SARANYA, ²P ROHITH SWARAJ, ³H ABHISHEK, ⁴B PRASAD SAI GIRI, ⁵V
KARISHMA, ⁶N AMULYA

¹Assistant Professor, Dept. Of EEE, DRK INSTITUTE OF SCIENCE & TECHNOLOGY, Hyderabad

^{2,3,4,5,6}BTech Student, Dept. Of EEE, DRK INSTITUTE OF SCIENCE & TECHNOLOGY, Hyderabad

Abstract: *Analyses of the Integrated buck-zeta converter in continuous conduction mode (CCM) are presented here. Rather of using a standard zeta converter, this one uses a buck converter. To elaborate, this circuit is based on the DISO zeta converter architecture, but it removes the H-bridge cell transistor and diode. Keeping the converter's number of parts to a minimum improves its performance. In contrast to multi-port buck-boost and cook topological, the output voltage polarity of both zeta and buck stages is positive. Serializing the input voltage sources is a key benefit of the integrated buck zeta converter, which leads to larger levels of DC voltage at the output, enhances reliability, and guarantees enough redundancy when compared to multi-port boost and SEPIC converters. Because of this, the converter may be used with reliable power sources. In the steady state, the converter's modeled state-space equations may be derived. The average current through an inductor and the average voltage across a capacitor may then be calculated by applying the averaging techniques to the state-space equations. Finally, the circuit is simulated in the MATLAB-Simulation environment to confirm the results of the analysis and computations.*

I. INTRODUCTION

In some applications, DC-DC typologies called multi input converters have several outputs to supply various electric loads simultaneously with different voltage levels. On the other hand, in other applications, such as uninterrupted power supplies, typologies named multi output

DC-DC converters require more than one input voltage source to ensure an adequate redundancy or increase

the overall input voltage level. The combination of these two types of converters yields multi-port DC-DC power

electronics converters (MIMOPEC), comprising several inputs and outputs. In other words, these converters have at least two input sources and two separate output electric loads. So, these converters are suitable candidates for uninterrupted power supplies as well as photovoltaic and fuel-cell fed systems [1], [3], [9]. These converters are designed based on either isolating methods, such as using

high-frequency transformers, or non-isolating methods, such as serializing/parallelization the voltage sources or using half bridge, full-bridge, and H-bridge cell typologies [1], [3], [5].

Two typologies have been used, based on the conventional buck-boost converter called DISO buck-boost and integrated buck-boost. Utilizing a first-order capacitor based filter in these converters increases the required capacitor size and makes the output voltage ripple proportional to the output load value [4], [5]. Furthermore, the input voltage sources cannot be serialized in the integrated buck-boost converter [5]. Also, the output voltage polarity of the integrated buck-boost converter is negative [4]. In an H-bridge cell-based boost, Cuk, and SEPIC, a

series induction should be dedicated to each voltage source, decreasing the converter efficiency and increasing the converter weight and size. Also, each voltage source should be connected to the circuit separately to energize the elements. So, it is not possible to increase the overall input voltage value by serializing the sources [1], [2], [9]. Finally, the complexity in use due to the arrangement of circuit transistors is a drawback of implementing DISO zeta and DIDO buck-zeta converters [2]. As a solution to the mentioned problems, the integrated

buck-zeta converter is introduced in this paper, along with the relating analyses at the continuous conduction mode (CCM). Two types of switching patterns can be applied to the circuit transistors to operate this converter: i) interleaved and ii) synchronized switching patterns [1]. Compared to the integrated DISO buck-boost converter, the output voltage value can be varied with less complexity [4], [5]. The second-order LC filters at the zeta and buck outputs make the voltage ripple in the voltage wave forms of both outputs independent of their electric loads. Also, the output voltage ripple of the zeta stage is less than that of any DISO buck boost

converters [1], [4], [5]. The ease in use and reduction in the number of components are other benefits of the integrated buck-zeta converter compared to the boost, Cuk, SEPIC, DISO zeta, and DIDO buck-zeta converters improving the converter efficiency and decreasing the circuit volume and manufacturing costs [1], [9]. The organization of this paper is given as follows: Section II describes the proposed topology. The steady-state analyses are given in Section III, while Section IV is devoted to simulations at CCM. Section V presents the conclusion.

II PROPOSED TOPOLOGY

The integrated buck zeta converter's schematic is shown in Fig. 1(a). This circuit uses a buck converter and a zeta converter, both of which are standard components. The buck converter in Fig. 1(a) consists of a modified H-bridge cell with one diode and one transistor, as well as an LC low-pass filter. H-bridge cell general schematic shown in Fig. 2(a).

The H-bridge cell may be simplified to lower power loss since the introduced topology is multi-input and unidirectional [1]. Thus, the switches and are superfluous.

Figure 2(b) shows the resulting simplified schematic. A transistor may be used to create the switch, and the switch can be used to

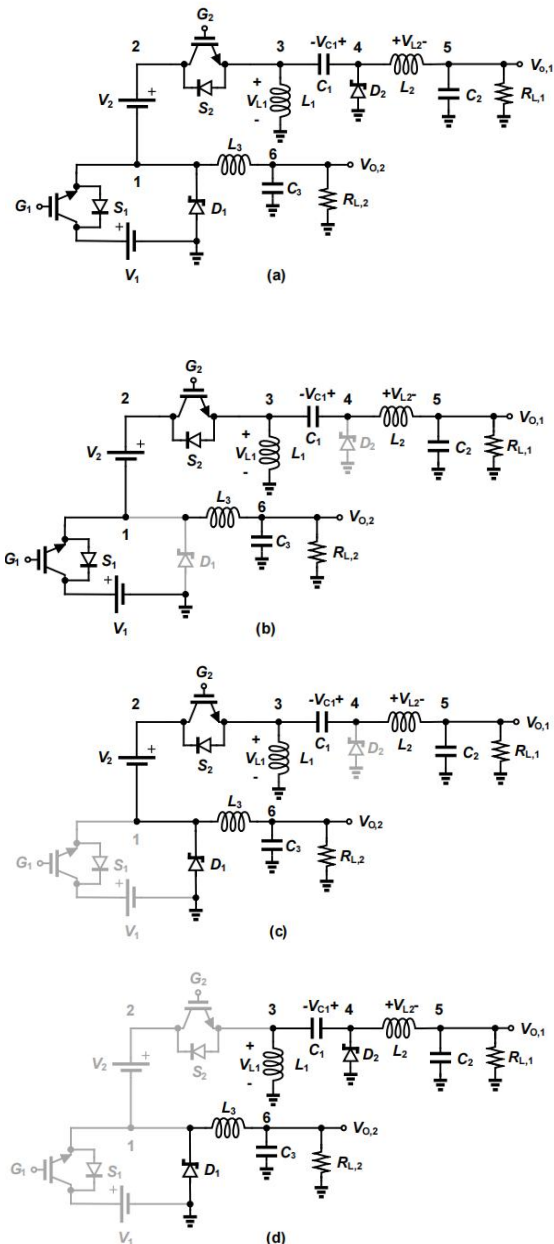


Fig. 1. Schematic of the proposed topology; (a) Circuit schematic, (b) Operation of the converter in mode 1, (c) Operation of the converter in mode 2, and (d)

Operation of the converter in mode 3.

III STEADY STATE ANALYSES

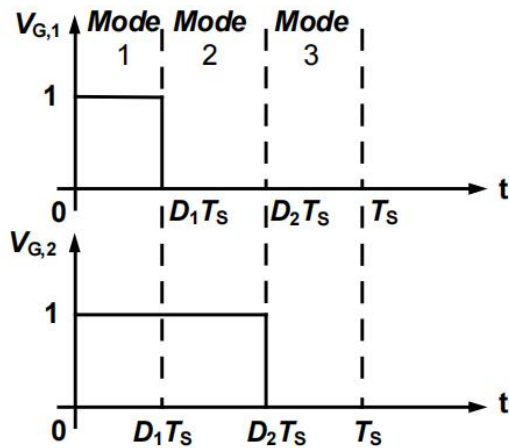


Fig. 3. Switching pattern diagram.

changed out with a diode [1]. Therefore, the transistor controls the voltage, while the diode allows the current to flow freely. The zeta stage is linked to the H-bridge cell's output. Therefore, the zeta stage receives electricity from two voltage sources, doubling the converter's dependability. The DIDO buck-zeta topology is modified by substituting a voltage source for the H-bridge cell2 to increase circuit efficiency [2]. In the input stage, where the H-bridge cell is located, the voltage source is always linked in series with the cell, meaning it cannot be removed or replaced. Therefore, it must be powered by a more stable voltage supply than the alternatives.

Activation Strategies

Two key assumptions, stated as follows, are required to streamline steady-state analyses:

It is assumed that all parts of the circuit are perfect and incur no losses.

The converter is run at CCM while the steady-state analyses are performed.

The suggested converter is a single H-bridge cell, as was indicated before [see Fig. 1(a)]. Fig. 3 is a diagrammatic representation of an appropriate switching pattern for use in the proposed circuit.

The converter may thus function in three distinct modes: i) when and conduct; ii) when and conduct; and iii) when and conduct, often known as the freewheeling mode. Notably, the formulae for the steady-state analyses are derived using the state-space averaging technique. As a result, we may define the matrices as:

$$\dot{X} = AX + BU \quad (1)$$

$$V_o = CX + DU, \quad (2)$$

where denotes the matrix of state variables, which includes voltages across capacitors and currents via inductors and is the

derivation matrix of the state variables. In this notation, and are the coefficient matrices of the state variables, and are the coefficient matrices of the independent input sources, and define the output variables matrix. [See Fig. 1(a)] The output variables are, respectively, and, so. Accordingly, the following are the available converter operating modes:

terval 0 o'clock. Input voltage sources and energy supply are shown in Fig. 1(b). The equations for the voltage across the capacitor and the current through the induction may be determined using KCL and KVL. Therefore, matrices representing states in state space may be written as

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_{L1}C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_{L2}C_3} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_1} \\ \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{1}{L_3} & \frac{1}{L_3} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & \frac{-1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_{L1}C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_{L2}C_3} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ I_{L3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_1} \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (5)$$

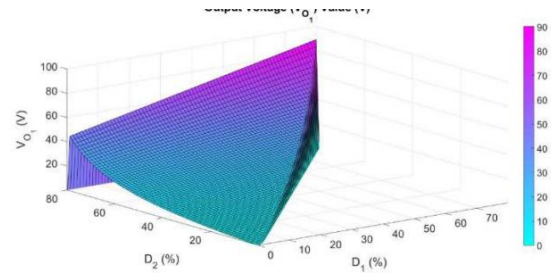


Fig. 4. Zeta stage output voltage contour plot.

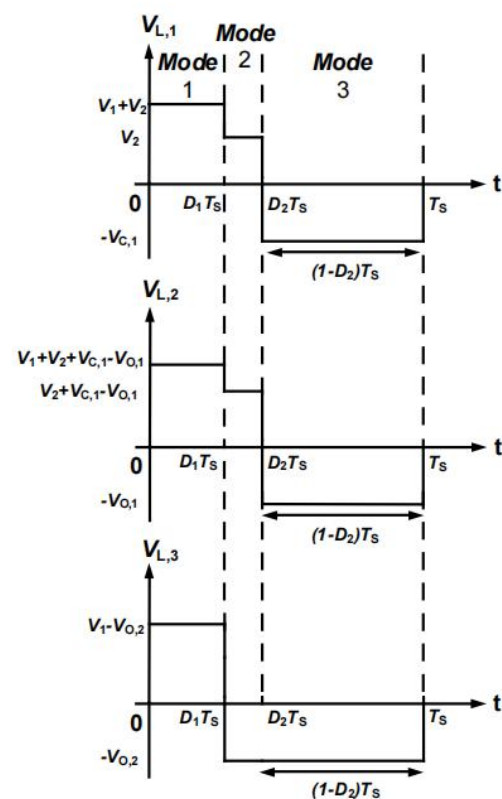


Fig. 5. The voltage wave forms of inductors.

can be calculated. Notably, the current wave forms of the inductors should be integrated over the interval to obtain the peak-to-peak current ripple [See Fig. 5].

Accordingly, the ripple in the inductor currents and capacitor voltages can be expressed as:

$$\Delta I_{L_1} = \frac{\bar{V}_{O_1}}{L_1}(1 - D_2)T_S \quad (18)$$

$$\Delta I_{L_2} = \frac{\bar{V}_{O_1}}{L_2}(1 - D_2)T_S \quad (19)$$

$$\Delta I_{L_3} = \frac{\bar{V}_{O_2}}{L_3}(1 - D_1)T_S \quad (20)$$

$$\Delta V_{C_1} = \frac{\bar{I}_{in}}{C_1}(1 - D_2)T_S \quad (21)$$

$$\Delta V_{C_2} = \frac{1}{8L_2C_2}T_S^2(1 - D_2)\bar{V}_{O_1} \quad (22)$$

$$\Delta V_{C_3} = \frac{1}{8L_3C_3}T_S^2(1 - D_1)\bar{V}_{O_2}. \quad (23)$$

IV SIMULATION RESULTS

Validating the formulas and theoretical calculations are done by simulating the proposed converter using the MATLAB-Simulation software. The converter is designed and simulated based on the component values illustrated in TABLE 1 to operate the circuit at CCM. Also, TABLE 2 presents the results of the theoretical calculations and simulations. The wave forms are depicted in Fig. 6 to Fig. 8, respectively. The zeta stage functions in the step-up mode. Fig. 6 shows voltage and current wave forms of the zeta stage input filter components. In (a) and (b), the voltage and current wave

forms of the capacitor are depicted, respectively. Also, parts (c) and (d) illustrate the inductor % voltage and

current wave forms, respectively. Fig. 7 depicts voltage and current wave forms of the zeta stage output filter components.

Hence, (a) and (b) exhibit the voltage and current wave forms of the capacitor and (c) and (d) show the inductor % voltage and current wave forms, respectively. Similarly, the voltage and current wave forms of the buck stage output filter components are depicted in Fig. 8; (a) and (b) demonstrate

the capacitor voltage and current wave forms, and (c) and (d) exhibit the inductor

% voltage and current wave forms, respectively. By considering the simulation results and the values given in TABLE. 2, it can be concluded that the

formulas are valid, and the converter operates at CCM.

V Conclusion

Operating the integrated buck-zeta converter has been proposed in this article. The behavior of the proposed converter was modeled by using the state-space equations and the averaging method. By

applying this method to the state space equations, formulas calculating the average current of inductors and the average voltage of capacitors are derived.

As a result, the average voltage of outputs and the average current of voltage sources can be determined. Meanwhile, the

simulation results validate the formulas and theoretical calculations. The output voltage ripple of the zeta stage is considerably less than that of the MIMO boost, Cuk, and SEPIC typologies. It is also independent of the load variation.

The ability to apply the input voltages in series makes it possible to achieve higher DC voltage levels at outputs compared to other multi-port converters, such as the boost, Cuk, and SEPIC. Besides, it can ensure adequate redundancy necessary in many applications. Compared to previous designs, reducing the number of circuit components improves the converter efficiency. Nevertheless, due to the discontinuity in the input current wave forms, the proposed topology may not be a suitable candidate for some renewable

TABLE 1. SIMULATION COMPONENT VALUE OF THE PROPOSED CONVERTER

Parameters	Value	Parameters	Value
V_1	12 V	D_2	52.8%
V_2	12 V	L_1	380 μ H
R_{L_1}	12 Ω	L_2	380 μ H
R_{L_2}	4.7 Ω	L_3	350 μ H
F_s	33.33 kHz	C_1	6.6 μ F
D_1	41.6%	C_2	6.6 μ F

TABLE 2. SIMULATION RESULTS OF THE PROPOSED CONVERTER

Parameters	Calculated Value	Simulated Value
\bar{V}_{O_1}	24 V	24 V
\bar{V}_{O_2}	5 V	5 V
ΔI_{L_1}	0.895 A	0.895 A
ΔI_{L_2}	0.895 A	0.895 A
ΔI_{L_3}	0.250 A	0.250 A
ΔV_{C_1}	4.8 V	4.8 V
ΔV_{C_2}	508 mV	508 mV
ΔV_{C_3}	142 mV	142 mV

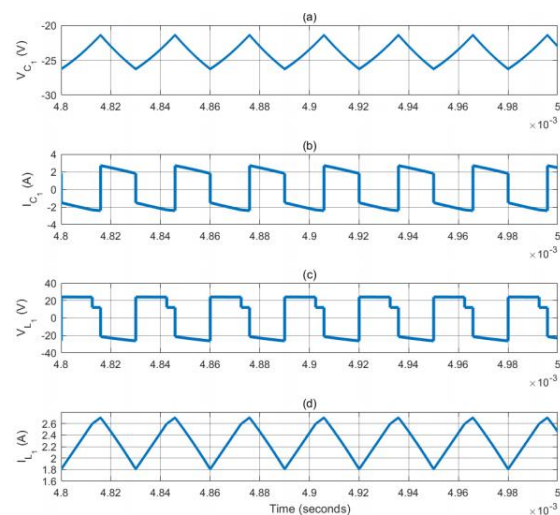


Fig. 6. Voltage and current wave forms of the zeta stage input filter (V_{C_1} and I_{C_1}) components. energy applications, such as PV installations. Accordingly, this converter can be appropriate for applications demanding high redundancy, reliability, and low output voltage ripple,

such as uninterrupted power supplies.

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