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# Design and Simulation of 10nm SOI TRI-Gate FinFET Using TCAD

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**Abstract-** Fin Field Effect Transistor (FinFET) has proven to be an alternative to the MOSFET in the development of low power analog and digital integrated circuits with lower short channel effects (SCE). This paper investigates the performance of a silicon-on-insulator based tri-gate FinFET modeled and simulated using TCAD virtual software. The SOI FinFET can provide performance improvement and ion/off ratio or leakage current reduction of more than two times for the same drive current compared to the bulk FinFET. The work function of aluminum (4.28eV) as gate metal has the lowest threshold voltage (0.1V) compared to the work functions of titanium (4.33), chromium (4.5), and molybdenum (4.6), which have progressively higher threshold voltages (0.19V, 0.2V, 0.25), respectively.

KEYWORDS:Fin Field Effect Transistor (FinFET), MOSFET, short channel effects (SCE), silicon-on-insulator (SOI), tri-gate FinFET, bulk FinFET

## 1. INTRODUCTION

The relentless quest for enhancing the performance of integrated circuits has led to the emergence of novel semiconductor technologies, with Fin Field Effect Transistors (FinFETs) standing out as a promising alternative to conventional MOSFETs. FinFETs have demonstrated remarkable potential in advancing both low-power analog and digital integrated circuits, primarily by mitigating short channel effects (SCE) inherent in traditional transistor designs.

This paper delves into the investigation of

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the performance characteristics of a Silicon-On-Insulator (SOI) based tri-gate FinFET, with a particular focus on its design and simulation using TCAD virtual software. The SOI FinFET architecture offers notable improvements, including enhanced performance metrics such as ion/off ratio and reduced leakage current, which surpass those achievable with bulk FinFET counterparts.

Through meticulous modeling and simulation methodologies, this study aims to elucidate the advantages of the 10nm SOI TRI-Gate FinFET configuration, shedding light on its efficacy in driving advancements in semiconductor technology. Moreover, the influence of different gate metal work functions, such as aluminum, titanium, chromium, and molybdenum, on threshold voltage and device performance will be explored, offering insights into optimizing transistor design for varied applications.

## 2. LITERATURE SURVEY

### *Multi-gate Mosfet Structures with High-k Dielectric Materials:*

Multi-gate MOSFETs have produced superior outcomes when used in subthreshold applications. It is possible to satisfy the requirements for multi-gate MOSFETS with a scaling trend in device size by substituting high-k dielectric for SiO2. The usage of several high K dielectric materials acting as oxide layers at different locations in MOSFET devices has increased as a result of advancements in fabrication technology. One among most significant multigate structures is the FinFET, which has demonstrated improved subthreshold swing (SS) and drain-induced barrier lowing (DIBL), both of which are made feasible by the ideal gate length to fin width ratio. In order to boost performance, we have covered various FinFET architectures in this study that make advantage of high K dielectric materials. Additionally, the efficiency of GAA with HfO2 gate oxide is examined and contrasted with that of conventional gate oxide. The strength of the fringing electric field is increased by using high-k dielectric materials like Si3N4 and HfO2. By lowering the off state current, sub threshold slope, and drain-induced FinFET barrier lowering while boosting the on state current, the device is improved. FinFET

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with high K dielectric. Material raises the Ion/Ioff ratio, expanding the potential for high Wfin Additionally, High K dielectric materials can be layered several times to improve performance in nanoscale applications.

**Subthreshold Characteristic Analysis and Models for Tri-Gate SOI MOSFETs using Substrate Bias Induced Effects:**

This paper proposes subthreshold models for tri-gate SOI MOSFETs (TGMOSFETs) for channel potential, threshold voltage, current, drain-induced barrier lowering, and subthreshold swing (SS). The resulting models additionally take into account the substrate-induced surface potential effect. A quasi-3-D method has been used to establish the minimum of the channel potential, which is then used to develop models of the threshold voltage, current, DIBL, and swing. The simulation outcomes from TCAD, have been compared to the simulated results of TG-SOI MOSFET. The subthreshold regime model, which takes into account For the conduction route potential, threshold voltage, current,

DIBL, and swing, substrate bias and SISP effect are produced. Substrate bias and the SISP effect are two additional factors that may be used to improve the Subthreshold current and SCEs in TGMOSFETs. The close resemblance of simulation data to the model, which includes the SISP parameter, V, ensures the model's validity and demonstrates that integrating the SISP effect in the boundary condition increases the model's accuracy

**Simulation Study of Hetero Dielectric Tri Material Gate Tunnel FET based Common**

**Source Amplifier Circuit:**

MOSFET has been supplanted by the tunnelling field effect transistor (TFET) in the creation of minimum power analogue and digital ICs. This essay evaluates the performance of a common source amplifier circuit built using a TFET device with a gate-all-around hetero dielectric tri material. The device is created using a look-up table-based Verilog and the Visual TCAD tool. An algorithm has been developed to simulate SPICE circuits. The performance of the HD-TMGTFET-based CS amplifier circuit is assessed in comparison to a MOSFET-based amplifier developed using 65nm MOSFET devices. In light of the

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device simulation's findings, The HD-TMGTFET device exhibits a high ON current of 7.5x10-6A/m, a low OFF state current in the order of 10-19A/m, and a steep subthreshold slope of 21.2 mV/decade. Additionally, the gadget displays incredibly low. In-depth analysis of designing common source amplifiers utilising the HDTMGTFET technology is provided in a publication. a circuit has been tested, and the outcomes of the simulation reveal that the suggested device shows incredibly better performance when creating circuits for analogue

applications. Any device that will be used to create high-performance, low-power VLSI circuits

should have strong ON current, extremely low OFF current, and a sharp sub threshold swing. The HD-TMGTEFT has exceptional performance in these areas. The device has high output resistance in the order of mega ohms and low miller capacitances Cgs and Cgd values. Maximum unity gain frequency is 124 GHz with a gate voltage of 0.9 V. indicating that the gate can withstand high frequency operation.

**Investigation of short channel effects in Bulk MOSFET and SOI FinFET at 20nm node technology:**

Multi-gate transistors were developed in place of planar bulk transistors in order to manage the SCEs in transistors that occur in the nanoscale and to increase performance. In this work, a 3D model of an SOI FinFET and a bulk MOSFET at a 20nm node technology is described along with its transfer characteristics, drain characteristics, and short channel effects. Calculations have been made regarding the threshold voltage, DIBL, and OFF state leakage current of SOI FinFET and bulk MOSFET. TCAD is used to simulate the device. According to the simulation results, SOI FinFET has a higher Ion than bulk MOSFET, and FinFET has a lower OFF state leakage current than bulk MOSFET. The SOI FinFET structure and the bulk MOSFET are created. Technology at the 20nm size and its transfer characteristics have been studied. It is discovered that the leakage current in the OFF state In addition to being less expensive than bulk MOSFET, SOI FinFET also lessens the short channel impact. This is due to its trigate structure, which offers greater channel control, and also to its

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incredibly thin body, which lowers leakage current compared to bulk MOSFET. Band-to-band tunnelling for both devices has been reported to cause the GIDL. It is shown that SOI FinFET is a potential device for scaling transistors into the nanoscale regime.

**FinFET Technology: As A Promising Alternatives for Conventional MOSFET Technology**

In the age of smart computing, memories occupy between 85 and 90 percent of the space in digital designs. Conventional MOSFET technology may be replaced with FinFET technology in digital logic circuits to lower power dissipation and enhance overall performance. Below 32nm, FinFETs are the greatest option to MOSFET technology since short channel effects may cause more issues. Almost all digital circuits now use FinFET technology instead of classic MOS due to its low leakage and low power features. In this research, it has been shown that FinFET technology is a good substitute for CMOS technology This leads us to the conclusion that the semiconductor industry is investigating cutting-edge methods for efficiently designing with FinFET technology. Scalability and energy efficiency are realated eachother.In the end, they are connected. The methods used for FinFET design and lithography are still not the most precise. It performs better than other planer transistor technologies, though. On the other hand, similar studies anticipate that the use of sub-5nm nanowire technology can address FinFET's drawbacks.

**Design and Simulation of 22nm FinFET Structure Using TCAD**

For the purpose of improving power and performance in the VLSI Optimising circuit, the FINFET concept is examined.The foundation for FINFET emerging technologies because of their performance, scalability, power efficiency, and improved control over short channel effects. In this study, the TCAD tool is used to analyse how the Hfo2 dielectric material affects the operation of FINFETs. The circuits' drain current is optimised by employing the high K dielectric material Hf02 The outcome demonstrates the enhancement in device performance while utilising different gate work functions (4.2ev to 4.6ev). The answer to high-optimizing gadgets will undoubtedly be better device structure.

TCAD software has been used to simulate

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and model a FINFET. Sio2 has limitations that must be addressed, although high dielectric constant materials. The structure has been modified to integrate Hfo2. The simulation demonstrates that FINFETs with Hfo2 as its dielectric material perform better in terms of drain current, proving that Hfo2 is the appropriate dielectric for the development of nanoscale device technology. The simulation research shows that increasing the efficiency of the currently in use metal gates may be accomplished by adjusting the threshold voltage in line with the metal gate work function. The metal gate work function in FINFETs can be properly adjusted to
reduce the short channel impact.

**Performance Enhancement of FinFETs at Low Temperature**

The three silicon temperature-dependent silicon piezoresistive coefficients have been used in this work to analyse the performance of strain-engineered MOSFETs. In order to explore the influence of stress-related effects, stress effects must be identified through simulation since stress has a significant impact on transistor properties in advanced devices. We looked into how low temperatures affected the electrical performance of FinFETs. The electrical properties of FinFETs are simulated and characterised using the physics-based 3D device simulation programme VictoryDevice. Performance is improved at low temperatures. The major goal of this research is to investigate the stress/strain contours in Si nanoscale FinFETs. A thorough investigation is conducted on the physical consequences of device strain. In the most advanced FinFETs, low temperature effects on electrical properties have been thoroughly explored. Several significant physical models were incorporated into device simulations, and we have examined the underlying device physics with regard to stress modelling. The simulation process and numerical approaches employed in VictoryStress were finally covered. For FinFETs, the results of process and device simulations are reported for various processing circumstances and the characteristics of the devices at low temperatures, respectively.

**Simulation study on FinFET with tri-material gate**

In this article, a novel tri-material gate

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(TMG) FinFET device is proposed. Using a three-dimensional (3-D) device simulator, the hot-carrier effects and short-channel effects of TMG FinFET are evaluated and contrasted with those of dual-material gate FinFET and conventional FinFET. Based on the findings of a numerical simulation, it can be seen that TMG FinFETs perform much better in terms of surface potential, electric field, and carrier velocity dispersion.recommended in this paper. Utilising a 3-D numerical device simulator, t TMG FinFET is examined. In terms of surface potential, carrier transport efficiency, HCEs, and DIBL, it is demonstrated that TMG FinFET performs better than DMG and SMG FinFET. Additionally, it is shown that a shorter L1 will result in a greater subthreshold current, whereas a longer M3 is required to suppress SCEs. . This research offers a flexible technique in addition to a new device structure.

**The Impact of Fin Number on Device's Performance and Reliability in Tri-gate FinFETs**

It was examined how performance and hot carrier-induced device degradation affected n-channel trigate multi-fin FinFETs with various fin counts. To ascertain the degree of device deterioration, the threshold voltage (VTH) shift, transconductance, and subthreshold swing degradation were retrieved. It was discovered that while devices with fewer fins perform better, they also experience more severe hot carrier-induced device deterioration. It is proposed that the multi-fin devices exhibit more dependability than single-fin devices under hot carrier stress because the coupling effect between the fins lowers the equivalent electric field in these devices. It was investigated how device characteristics and hot carrier-induced FinFET degradation with various fin counts interact. Because of this, FinFETs with fewer fins perform better, but they also degrade more quickly when subjected to HCI stress. Every fin in the multi-fin FinFET is in close proximity to one another, which causes charges to reject one another and further reduces the inversion charges in the centre fin. This suppresses impact ionisation and lowers the hot carrier-induced degradation.

**Simulation and Optimization of Tri-Gates in a 22 nm Hybrid Tri-Gate/Planar Process**

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3-D device simulations (Sentaurus D-2010) were used to examine a Tri-Gate structure included into a planar 22 nm bulk process. All implants were shared as was possible while processing planar and Tri-Gate CMOS simultaneously, with the exception of an extension of the planar process flow sequence to include additional Tri-Gate patterning. Comparing planar and Tri-Gate transistors with he same planar dopant profiles reveals that Tri-Gates have significantly improved subthreshold
slope, DIBL, and VT-rolloff. It has been investigated how different Tri-Gate heights and widths affect
the Tri-Gate transistor's electrical behaviour. Electrostatics and ION-IOFF properties performed
better in a vast space of Tri-Gate dimensions than on a planar surface.

Tri-Gate strategy with a planar process beginning has been assessed for ITRS technology assumptions
of 22 nm. A low-cost Tri-Gate/planar hybrid technology is based on such an approach, with Tri-Gates
and planar would utilise the identical dual band-edge metal gate workfunctions, implant masking, and
S/D procedures. According to 3-D simulations, Tri-Gate NMOS perform much better in terms of
electrostatics and ION-IOFF than a planar NMOS with the same dopant profiles and gate oxide
thickness. It has been proven that there is a sizable design space with Tri-Gate dimensions that
performs better than planar

**EXISTING SYSTEM:**

Prior to the advent of the 10nm SOI TRI-Gate FinFET, the semiconductor industry heavily relied on conventional planar MOSFETs to construct integrated circuits, owing to their established performance and reliability. These MOSFETs, with their flat architecture, have been fundamental in powering electronic devices for decades. However, as technology progressed and the demand for smaller and more efficient devices grew, conventional planar MOSFETs encountered several limitations.

As transistor dimensions were scaled down to meet the demands of Moore's Law and the pursuit of higher integration densities, conventional planar MOSFETs encountered

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significant challenges. One of the primary issues was the increasing difficulty in maintaining performance and power efficiency at smaller scales. With the shrinking of transistor dimensions, phenomena such as short-channel effects became more pronounced, leading to performance degradation and increased power consumption.

Furthermore, conventional planar MOSFETs faced limitations in achieving higher transistor densities due to physical constraints associated with their flat structure. This limitation hindered the realization of more complex and feature-rich integrated circuits, thereby impeding the advancement of electronic devices.

Moreover, as transistor sizes decreased, issues related to leakage currents became more pronounced. Leakage currents, which occur due to quantum mechanical effects at smaller scales, contribute to wasted power and reduced battery life in portable devices. Additionally, the inherent speed limitations of conventional MOSFETs posed challenges in achieving faster processing speeds, limiting the overall performance of electronic devices. In terms of manufacturability, conventional planar MOSFETs faced challenges in adapting existing manufacturing processes to produce devices with smaller node sizes. This resulted in lower yield rates and increased error rates during production, further exacerbating the limitations of the existing system

**DISADVANTAGES OF EXISTING SYSTEM:**

1. Conventional planar MOSFETs struggle to maintain performance and efficiency as transistor sizes decrease.

2. architecture hampers achieving higher transistor densities, limiting integration capabilities.

3. Shrinking transistor dimensions exacerbate leakage current issues, impacting power efficiency and battery life.

4. Existing processes may not suitably adapt to produce smaller devices, leading to lower yields and higher error rates.

**PROPOSED SYSTEM:**

The proposed system focuses on the design and simulation of a 10nm Silicon-on-

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Insulator (SOI) Tri-Gate FinFET utilizing TCAD virtual software. This project aims to address the limitations of conventional planar MOSFETs prevalent in the semiconductor industry. By leveraging emerging technologies and innovative transistor architectures, the proposed system endeavors to significantly enhance the performance, power efficiency, and manufacturability of electronic devices.

Key objectives include the implementation of an advanced three-dimensional transistor structure, which enables better electrostatic control and mitigates short-channel effects. Through meticulous design and simulation processes, the proposed system aims to achieve higher transistor densities, faster processing speeds, and reduced leakage currents compared to traditional MOSFETs. Moreover, by optimizing power efficiency through the unique characteristics of FinFETs, such as reduced subthreshold leakage and improved gate control, the proposed system seeks to prolong battery life in mobile devices and decrease energy consumption in computing systems.

Furthermore, the project emphasizes the importance of enhancing manufacturability. By developing manufacturing techniques tailored to produce smaller node sizes, the proposed system aims to ensure high yield rates and minimize errors during production. Overall, the 10nm SOI Tri-Gate FinFET project promises to usher in a new era of semiconductor technology, enabling the development of more efficient, powerful, and reliable electronic devices.

**ADVANTAGES OF PROPOSED SYSTEM:**

Increased transistor density: By packing a greater number of transistors into a single semiconductor with a lower node size, performance and functionality may be improved. This enhanced density enables the integration of more components on a chip, leading to increased computational power and enhanced functionality in electronic devices.

Increased power efficiency: The distinctive structure of FinFETs, particularly the Tri-gate FinFET, allows for a reduction in power usage compared to conventional planar MOSFETs. This reduction in power

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consumption can potentially extend the battery life of mobile devices, offering users longer usage times without the need for frequent recharging.

Increased speed: Transistors tend to turn on and off more quickly as their size decreases. Therefore, with the smaller size of a 10nm SOI Tri-gate FinFET, faster processing speeds can be achieved in computer devices. This speed enhancement contributes to improved overall performance and responsiveness in electronic systems.

Reduce leakage current: As transistors become smaller, they tend to leak more current, which can negatively impact power efficiency and device reliability. By utilizing a 10nm SOI Tri-gate FinFET, it is possible to mitigate this issue by reducing leakage current, thereby enhancing power efficiency and device dependability.

Enhance manufacturability: The development of a 10nm SOI Tri-gate FinFET requires the utilization of new manufacturing techniques to accommodate the smaller node size and complex three-dimensional structure. One of the primary goals of these manufacturing advancements is to optimize the production process, ensuring high yield rates and minimizing errors. This enhanced manufacturability contributes to the scalability and viability of the technology for mass production in the semiconductor industry.

## 3. RESULTS:

This section discusses the TCAD tool's simulation findings that were attained following the creation
of the device. The Id Vs Vg characteristic curve has been plotted in accordance with the results of a
complete simulation carried out at room temperature with a supply voltage of 1V.
The gate voltage, temperature, and doping profiles are just a few of the variables that will affect the
IV (current-voltage) characteristics of an SOI Tri-gate FinFET with a channel length of 10 nm.The
relationship between the drain current (I_D) and drain-source voltage (V_DS) at a fixed gate voltage
(V_G) is depicted by the IV characteristics

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curve. Typically, the curve comprises three regions:

Ohmic region: The current grows linearly with voltage in this region. The channel resistance, which

is inversely correlated with the channel length, determines the slope of the curve.

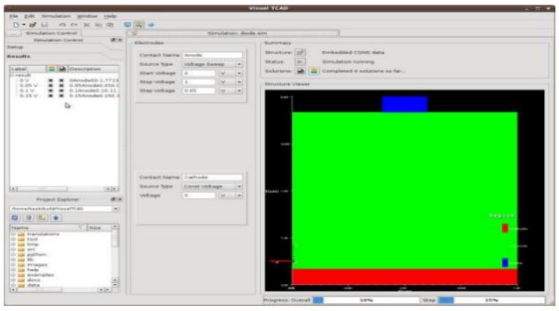
Saturation region: The current achieves its greatest value in this zone and does not rise with voltage.

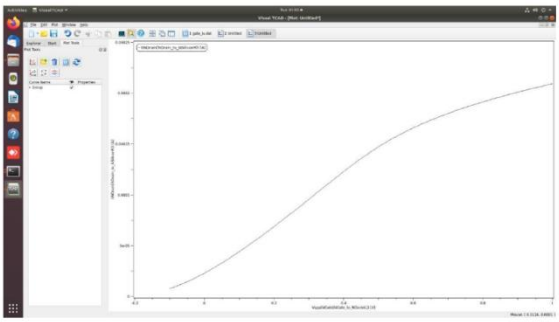
Carrier velocity saturation and channel gate control both set a maximum current limit.

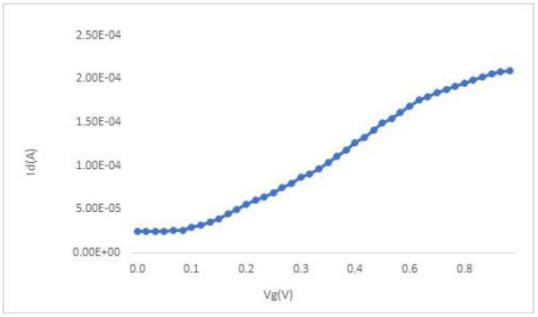
Subthreshold region: The current is extremely low in this region and rises exponentially with

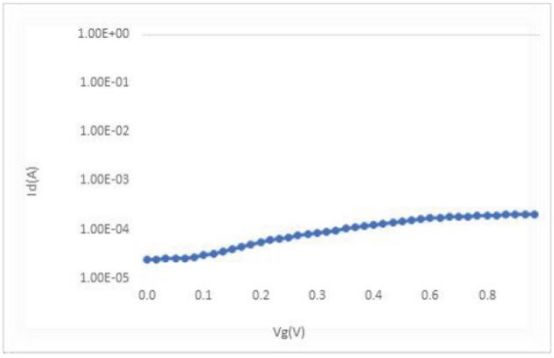
voltage. The subthreshold swing and threshold voltage are determined by this region, which is crucial

for low-power applications.








| Gate Material | Work function(eV) | Threshold voltage(V) |
|---|---|---|
| Aluminum (Al) | 4.28 | 0.13 |
| Titanium (Ti) | 4.33 | 0.19 |
| Chromium (Cr) | 4.5 | 0.2 |
| Molybdenum (Mo) | 4.6 | 0.25 |

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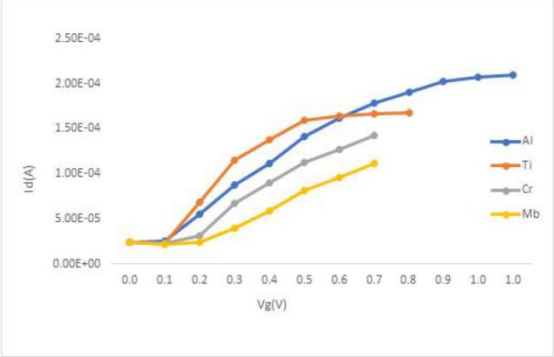


## 5. CONCLUSION

In the virtual TCAD, a silicon-on-insulator based tri gate FinFET is designed and simulated. The SOI

FinFET can deliver a performance improvement and an Ion/Ioff ratio advantage compared to bulk

FinFET, or a reduction in leakage current of almost two times at the same drive current.

It is obvious from the simulation research that adjusting the threshold voltage in accordance with the

work function of gate metal improves the usage of metal gates. Additionally, the short channel effect

in FINFETs may be strengthened by correctly modifying the metal gate work function.

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